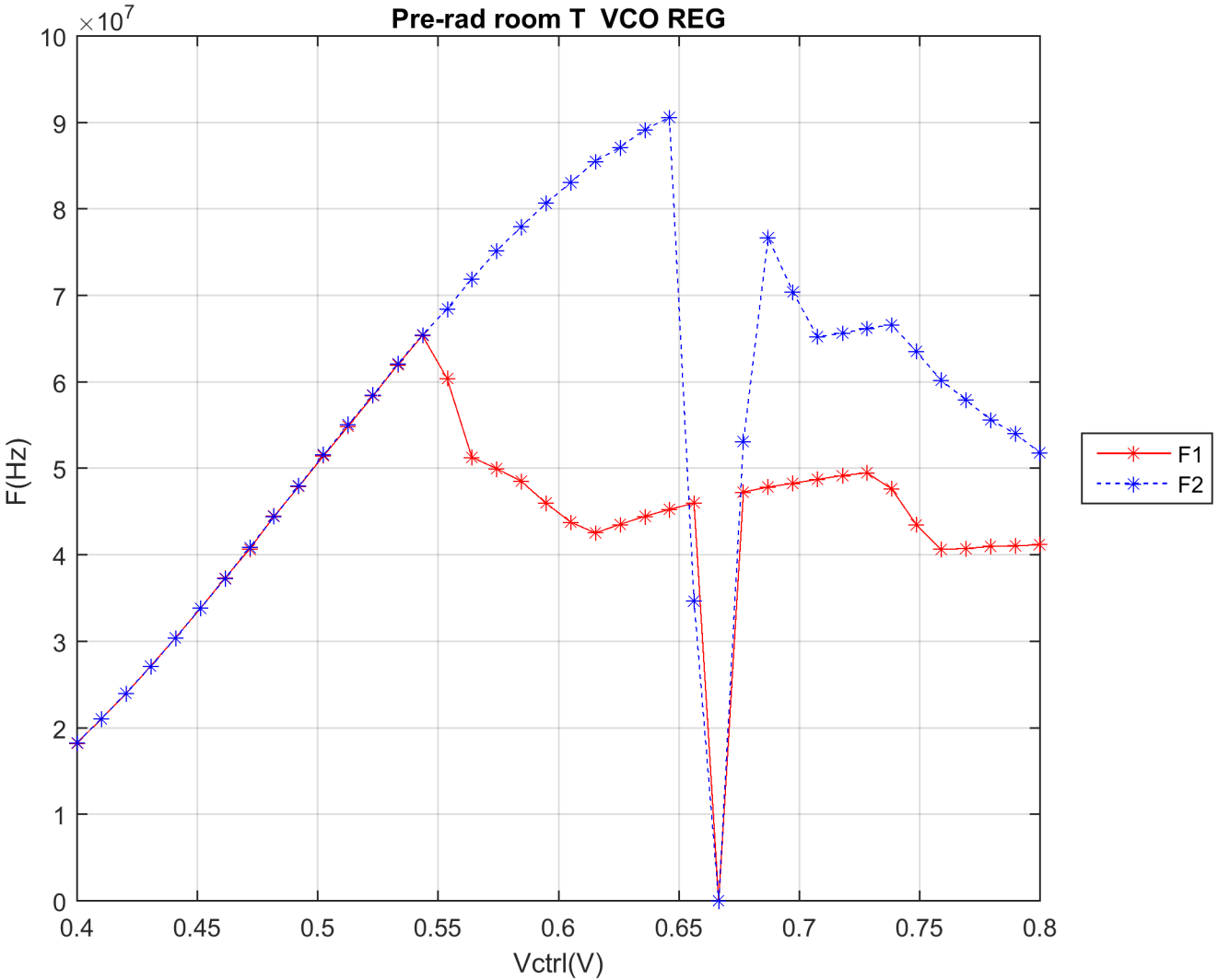
EXPERIMENT: 200Mrads at room temperature:

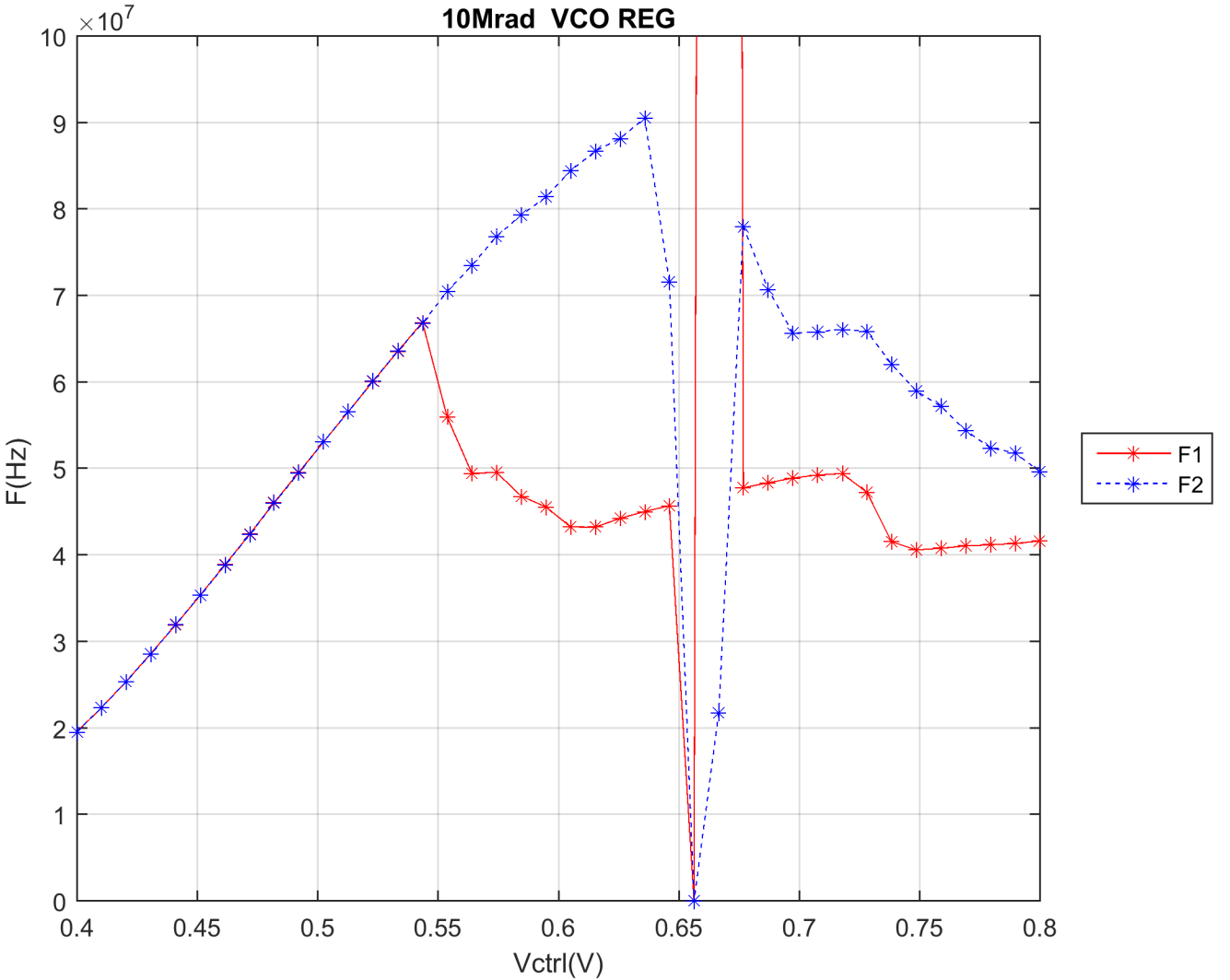
OVERVIEW:
1st. Irradiation at room temeprature, up to 200Mrads.
2nd. Room temperature annealing for one week.
3rd. High temperature annealing, 100C, 3 days.
As the chip was not working at high temperature, every measurement in this step was taken cooling down the chip (going to room temeprature).

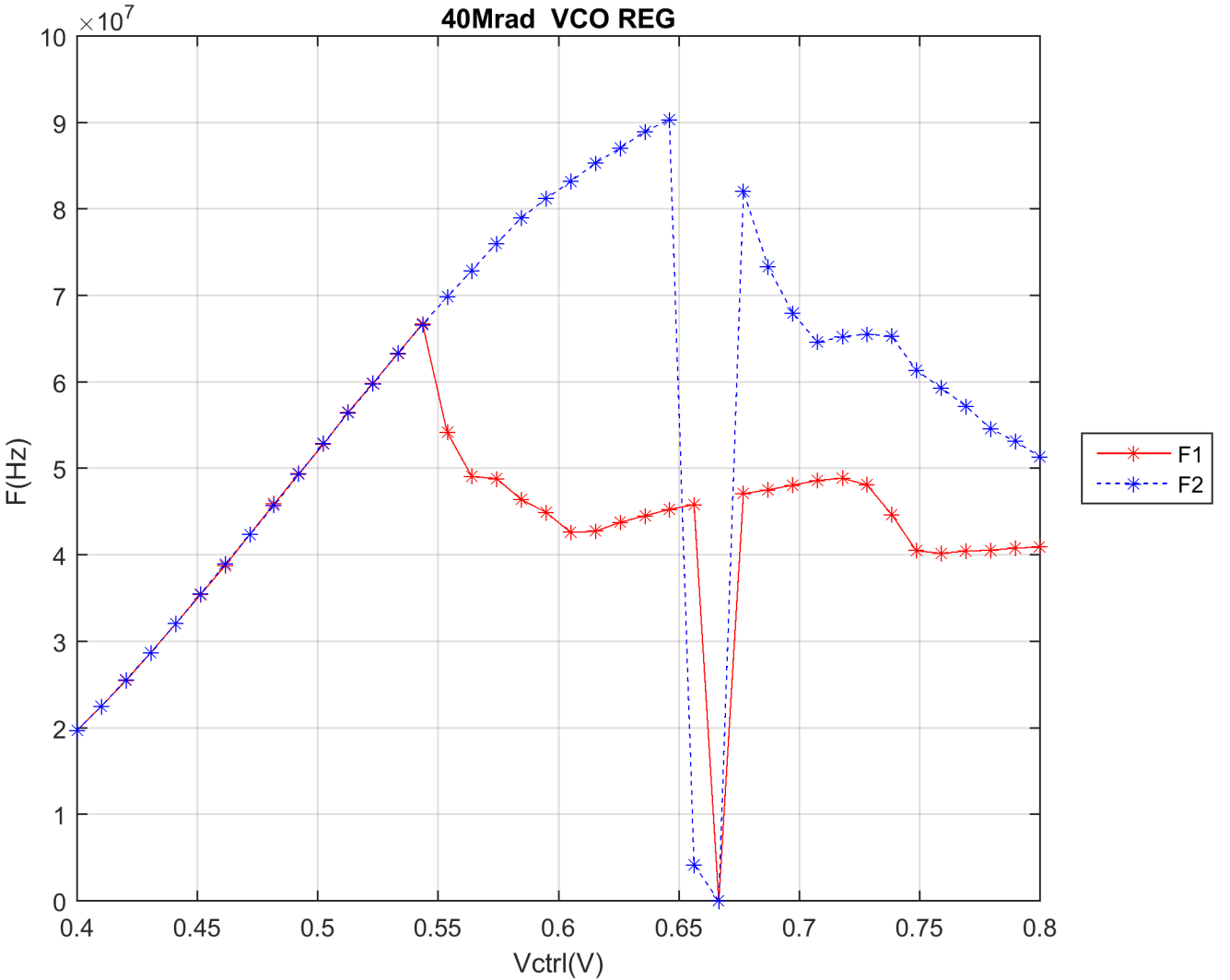
Results of three tests are included, reapeted for several TID and in different time stamps during annealing:
1. Vctrl sweep for REG transistors VCO (measuring the frequency vs Vctrl).
2. Vctrl sweep for ELT transistors VCO (measuring the frequency vs Vctrl).
3. Skip test for ELT transistor VCO.The voltage used for the VCO (Vctrl) in the skip test depends on the results obtained in 2: it uses the voltage needed in 2 to reach around 50MHz (the software reads the results of the previous test and it takes the Vctrl that makes the VCO oscillate with the closest frequency to 50MHz but always below 50MHz).

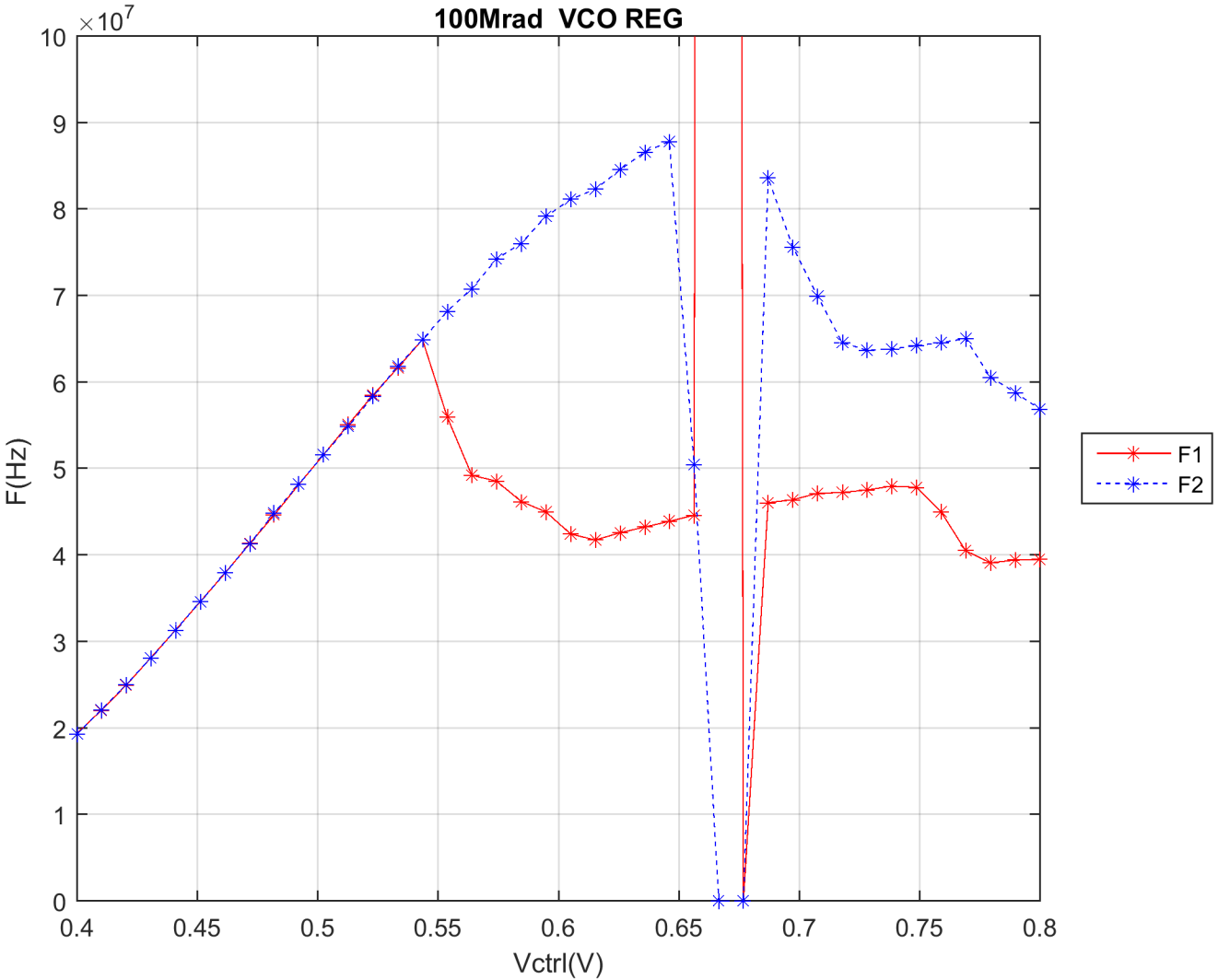
? (More data is available for other TIDs, here only some of the points are shown).

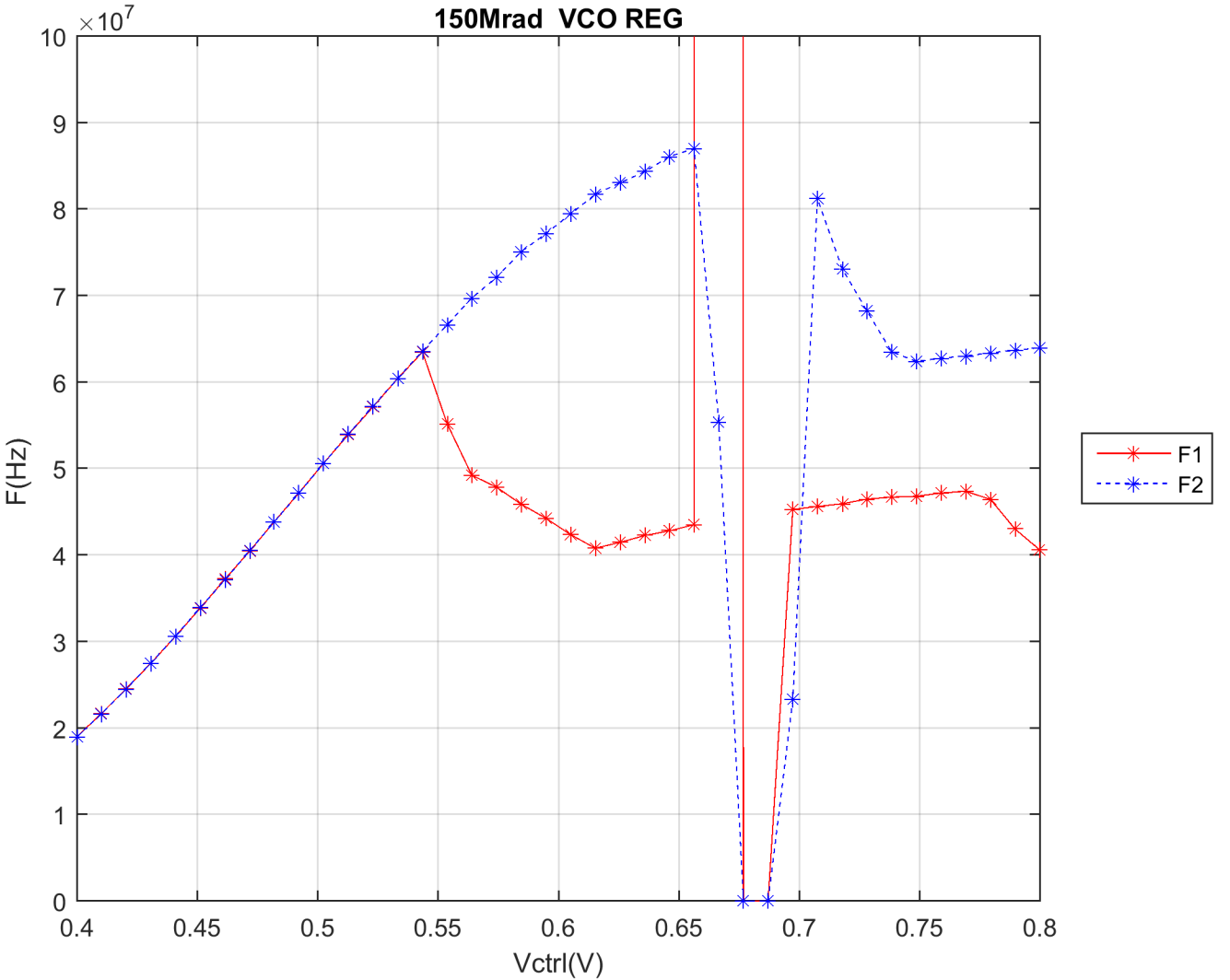
1. Vctrl sweep for REG transistors VCO (measuring the frequency vs Vctrl).

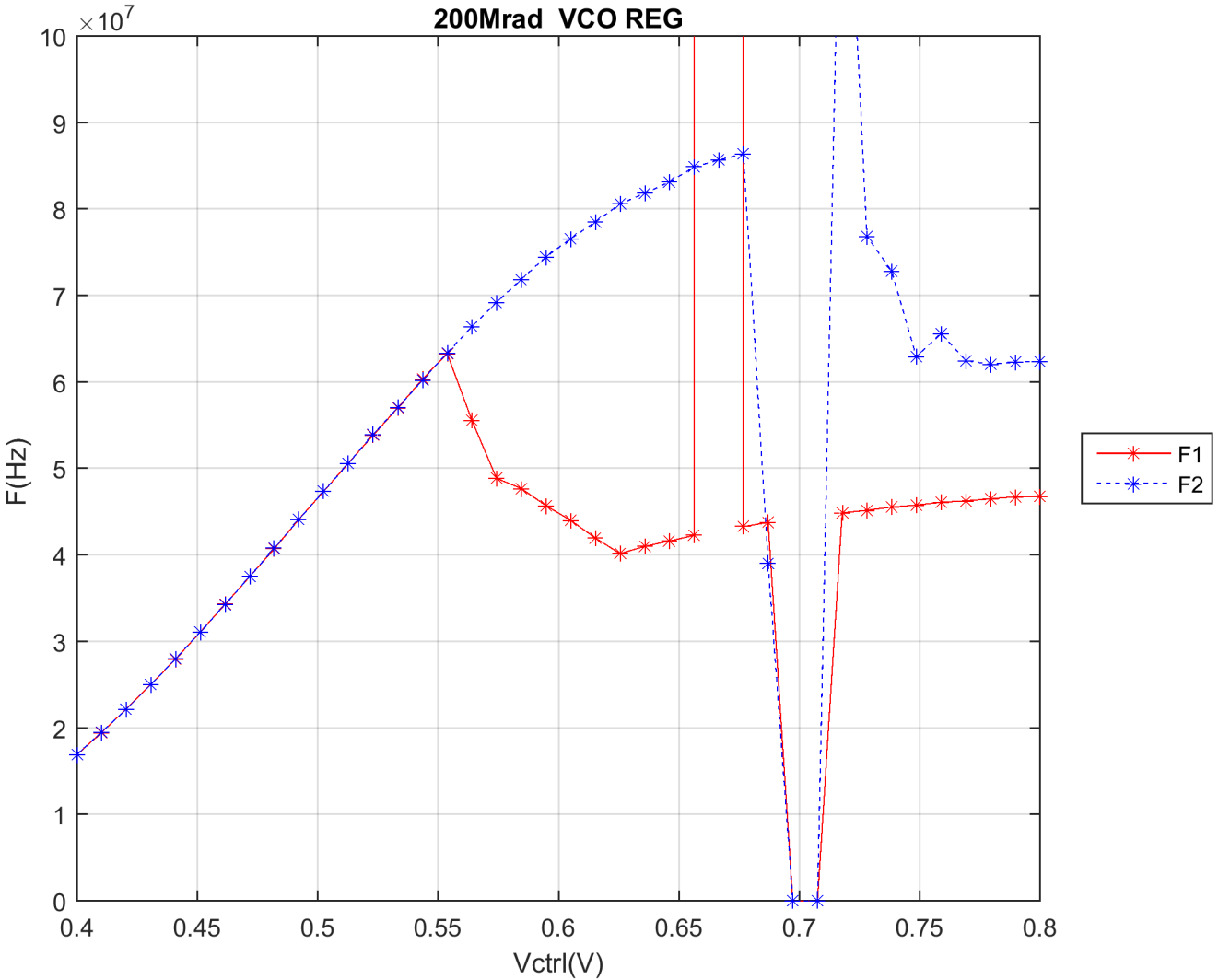

Pre-rad room T VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

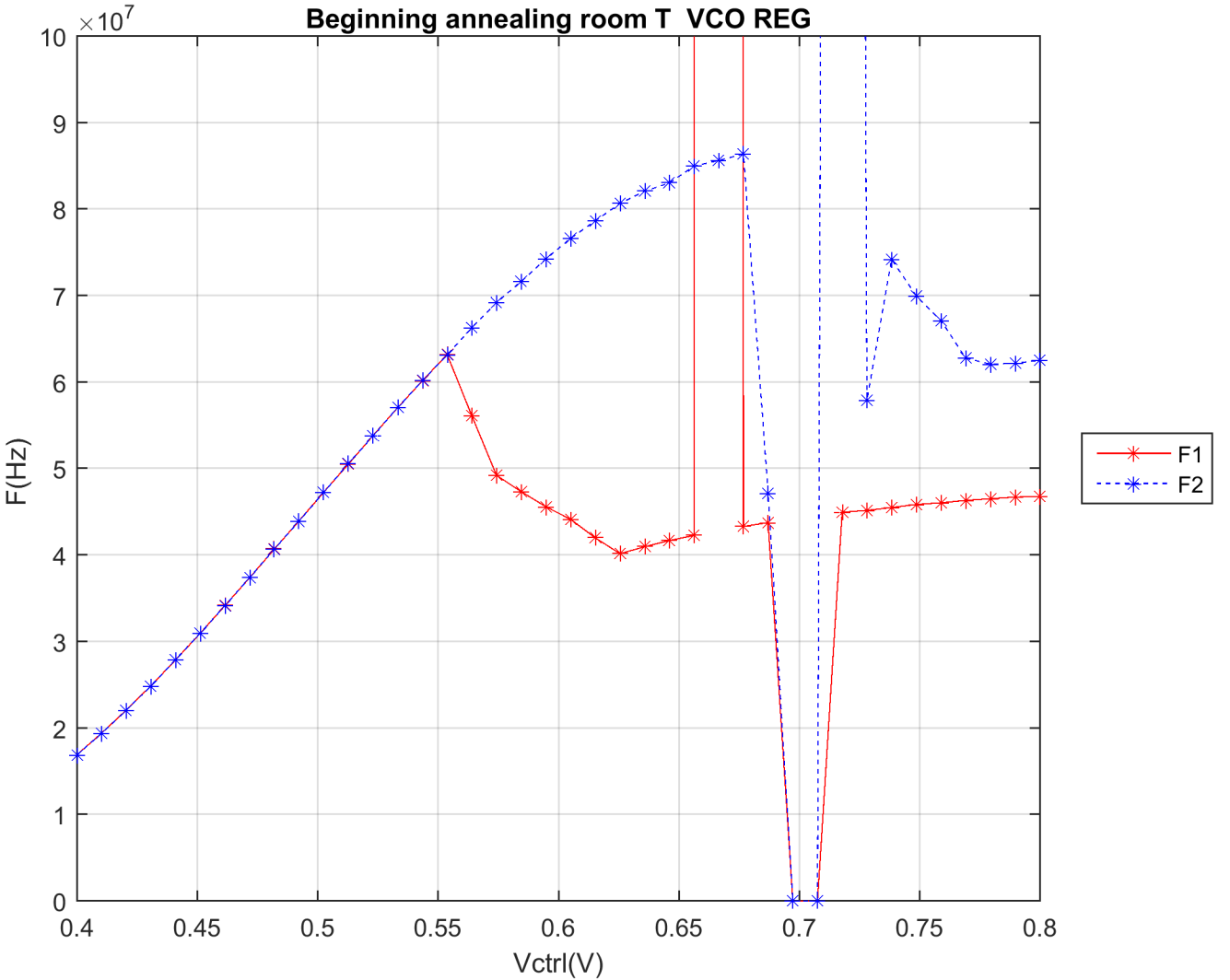

10Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

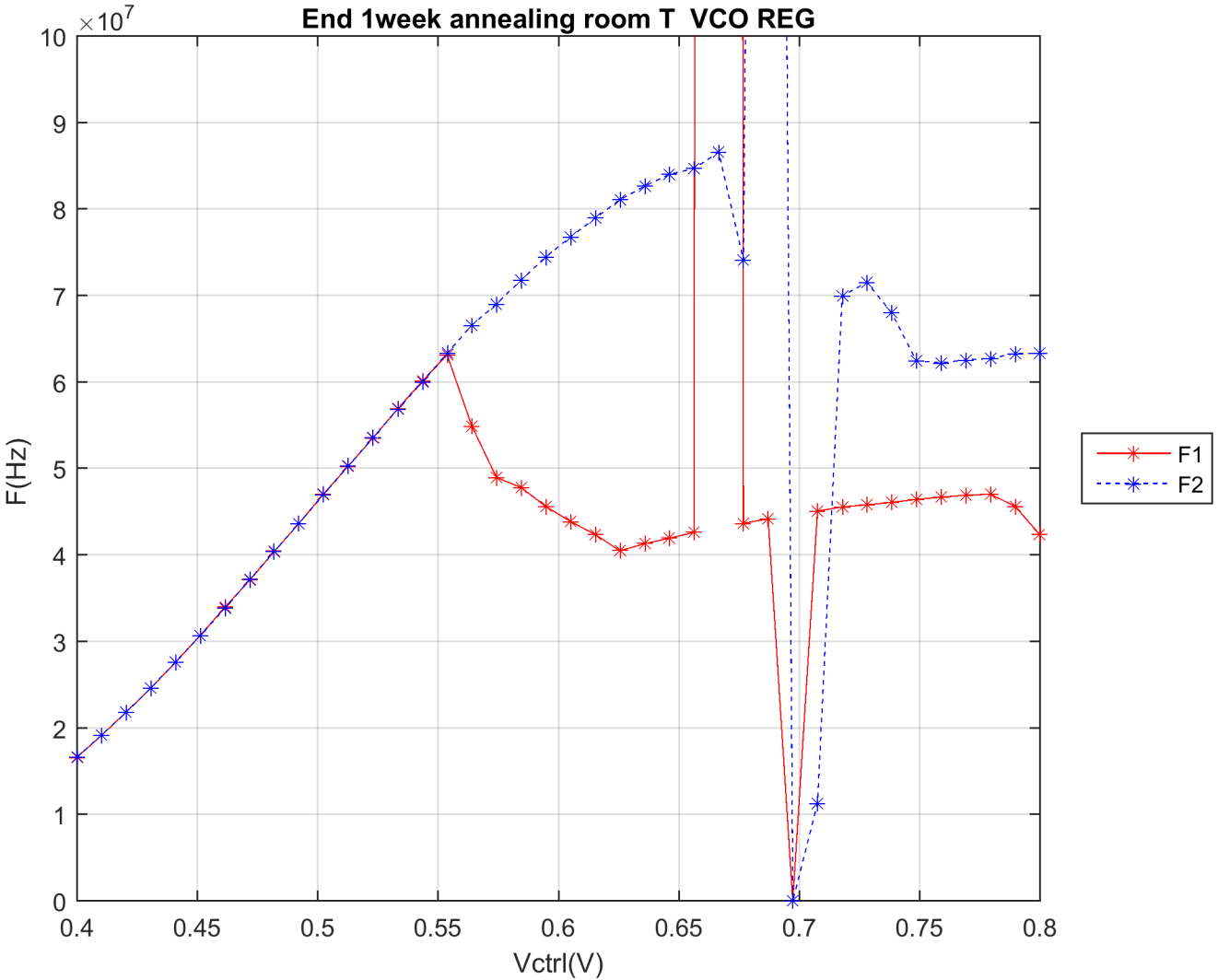

40Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

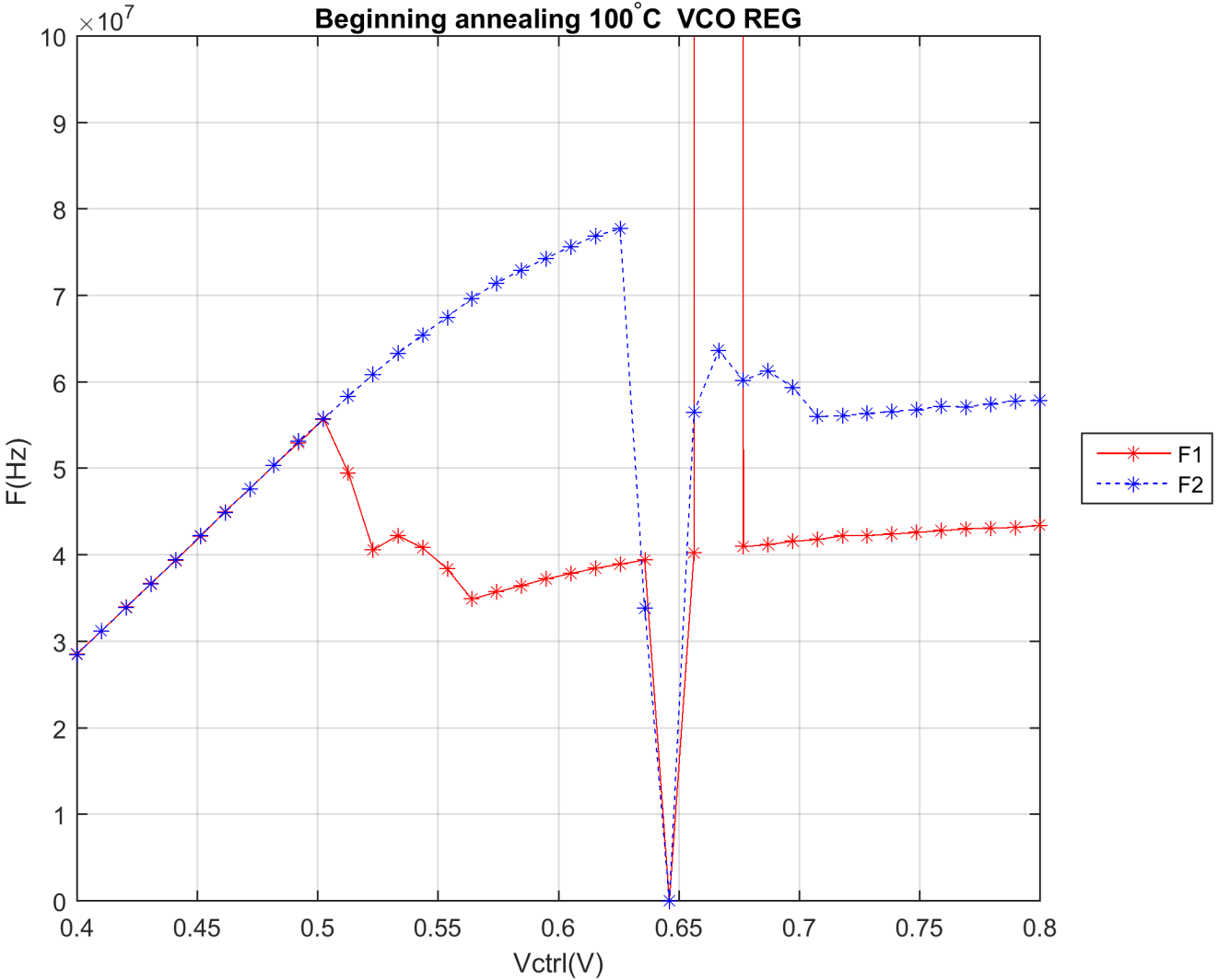

100Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

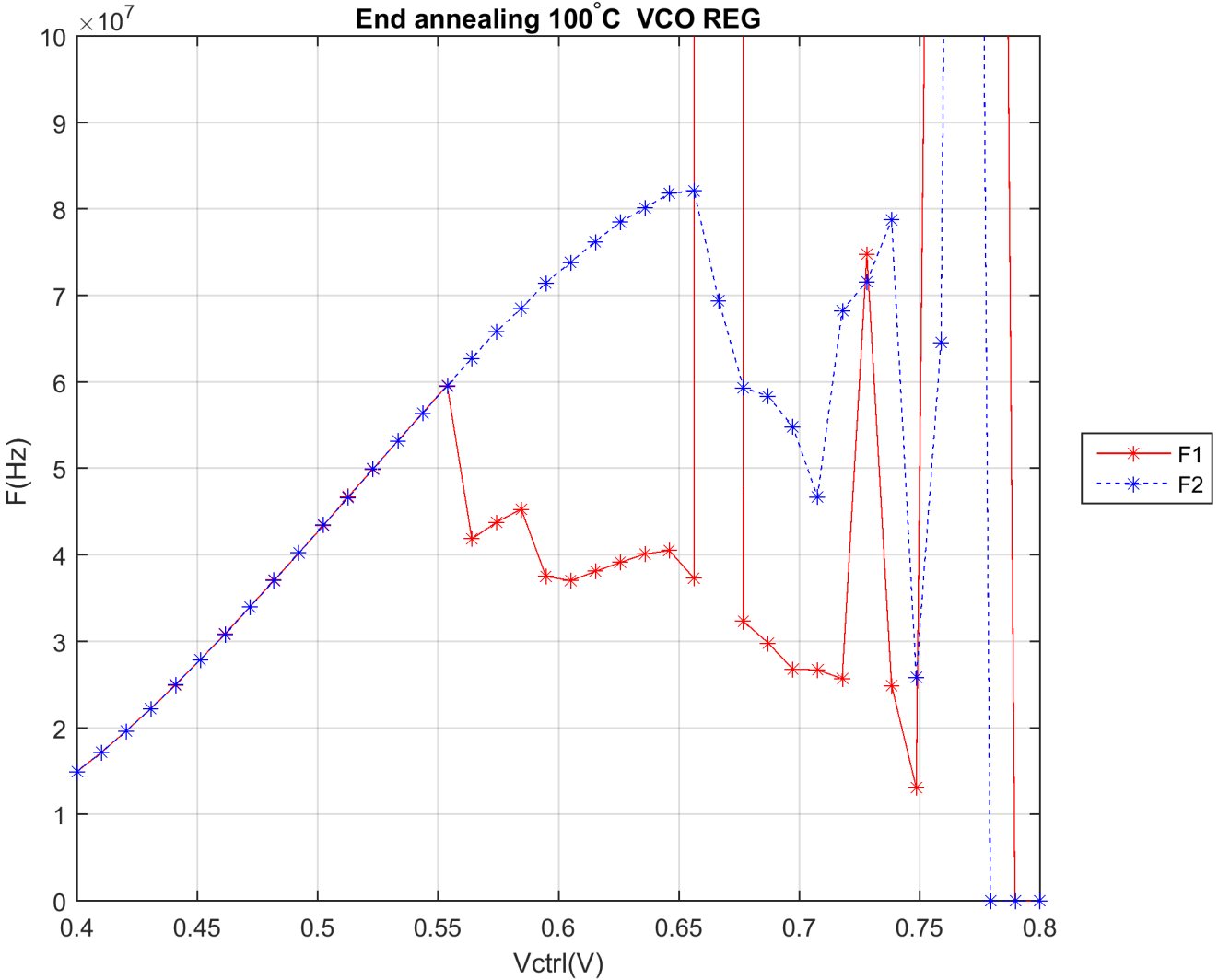

150Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2


200Mrad VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

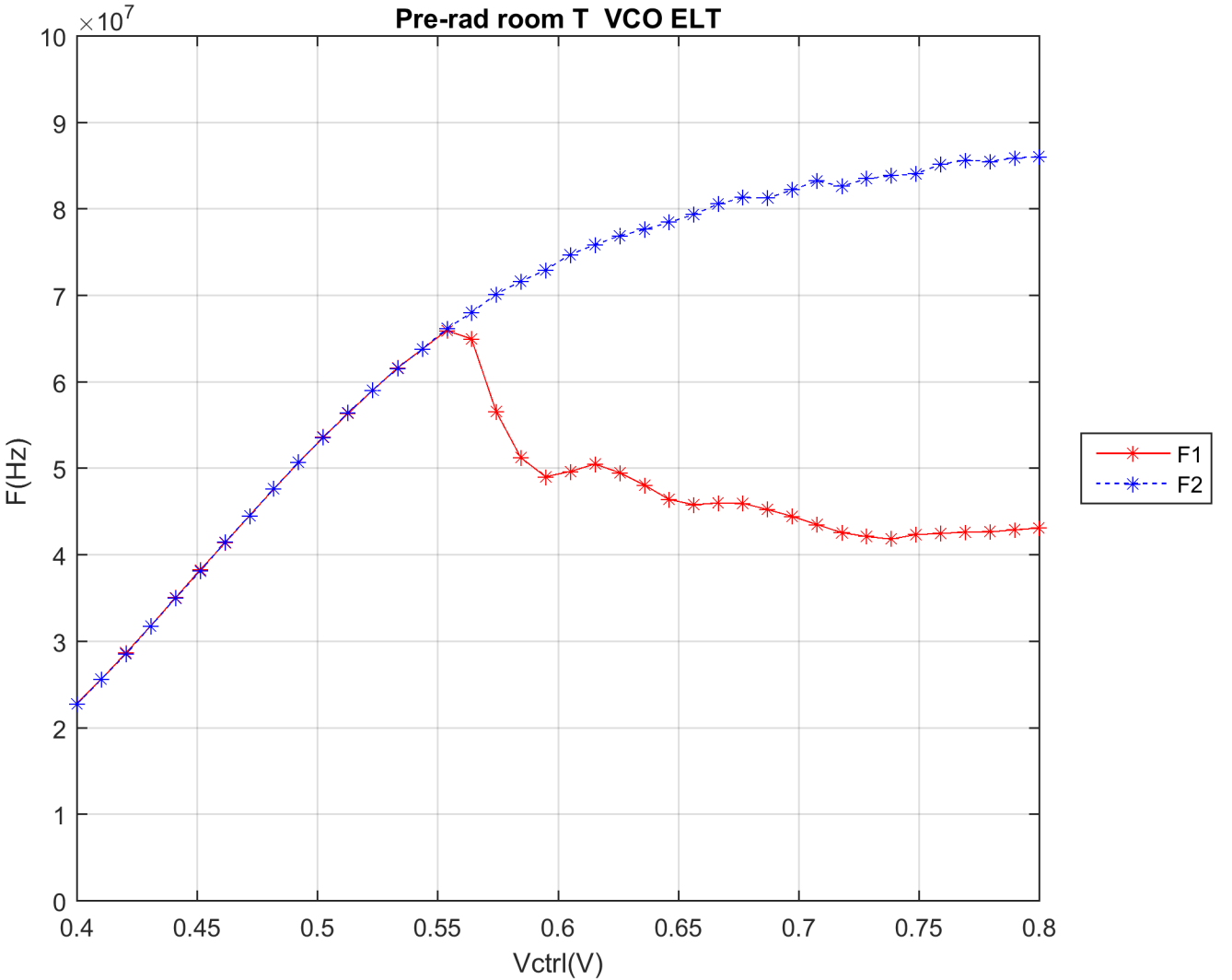

Beginning annealing room T VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

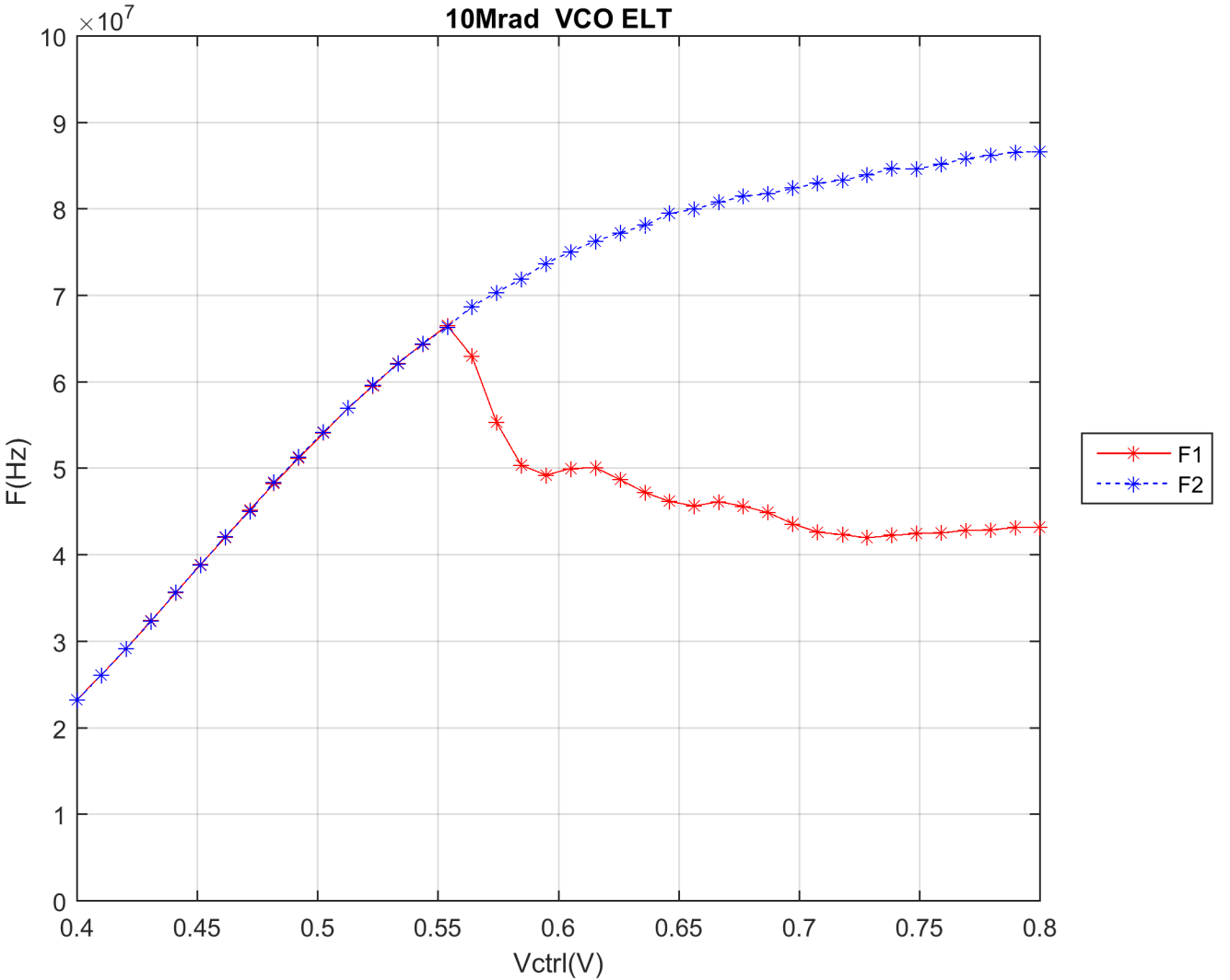

End 1week annealing room T VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

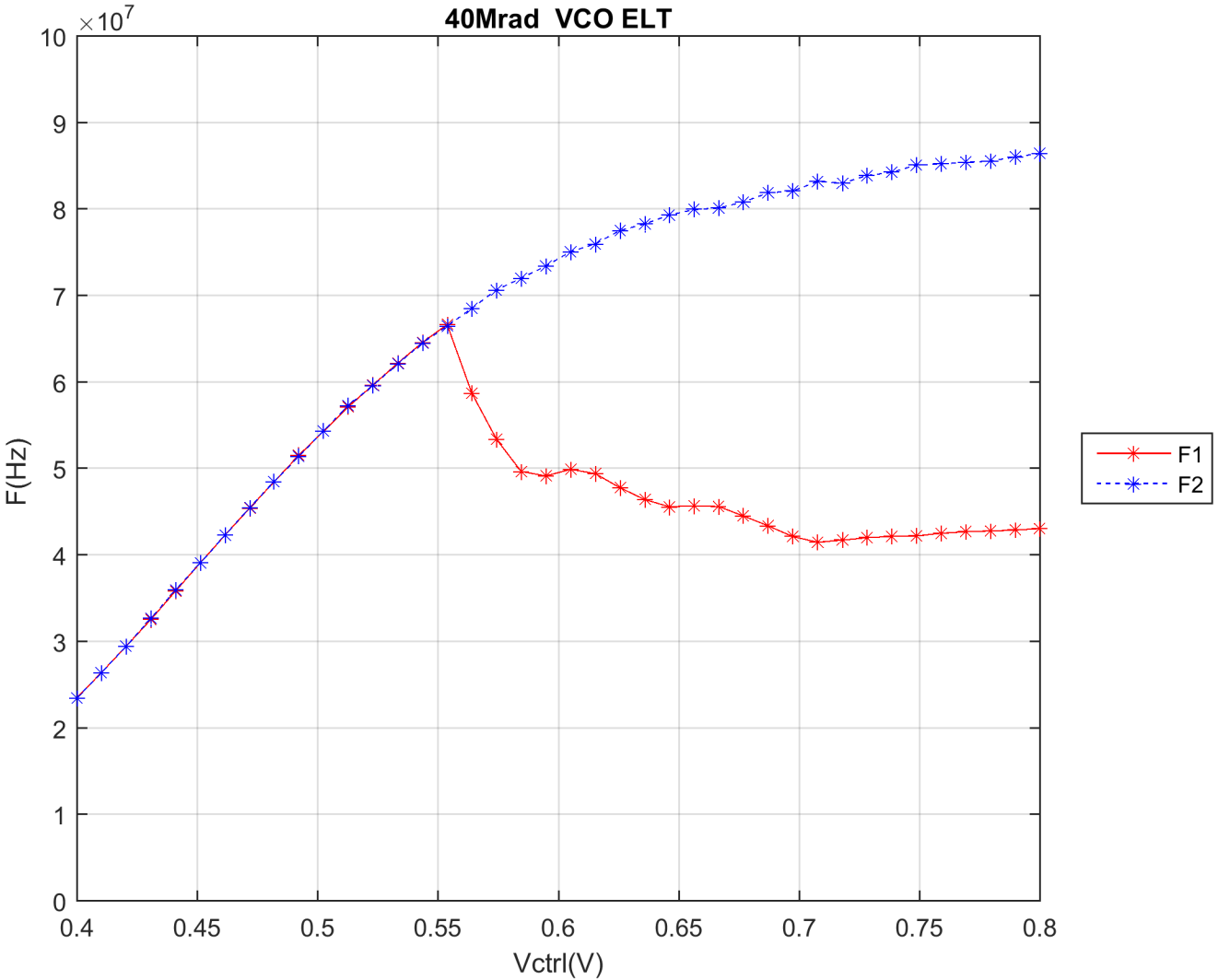

Beginning annealing 100°C VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

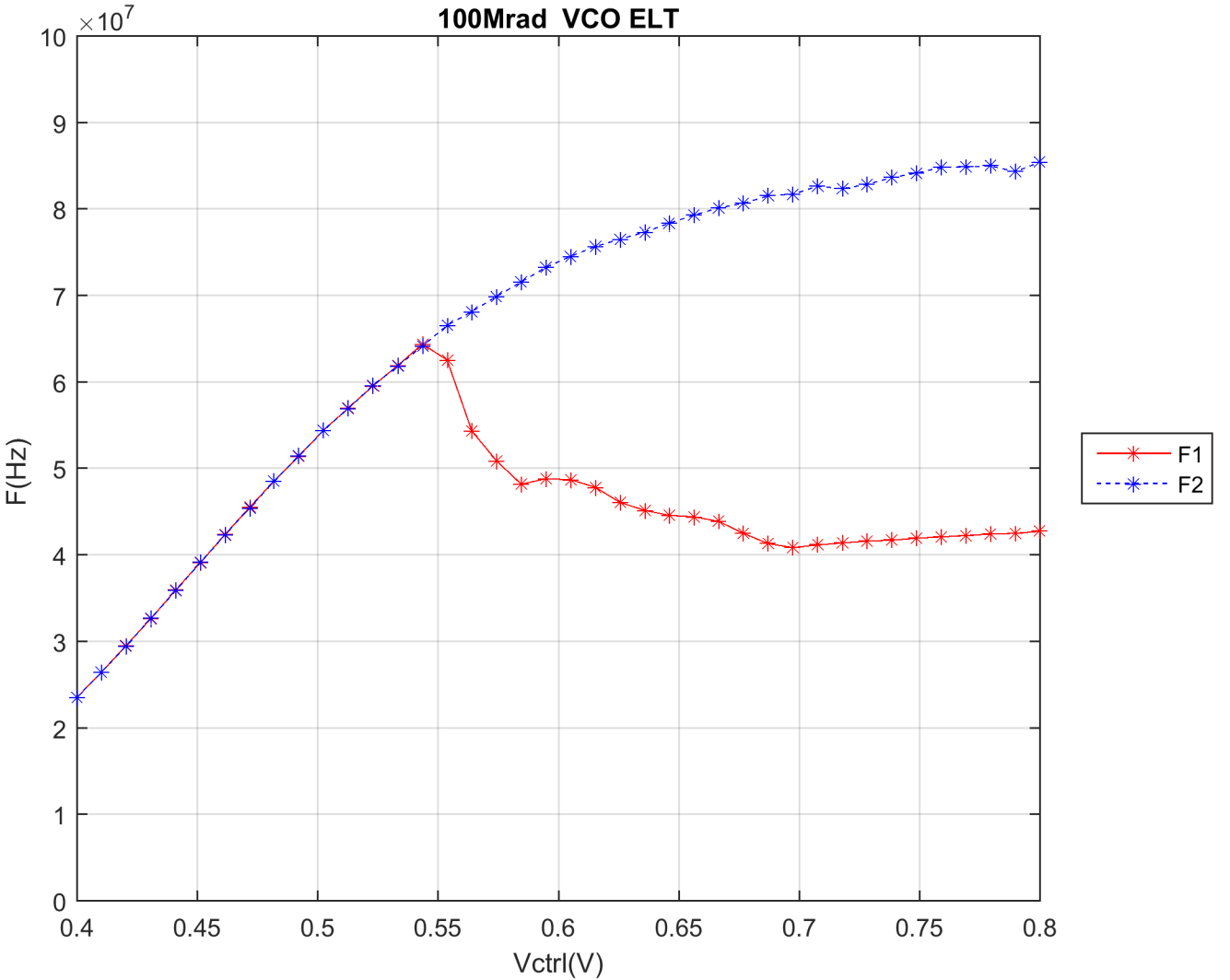

End annealing 100°C VCO REG
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

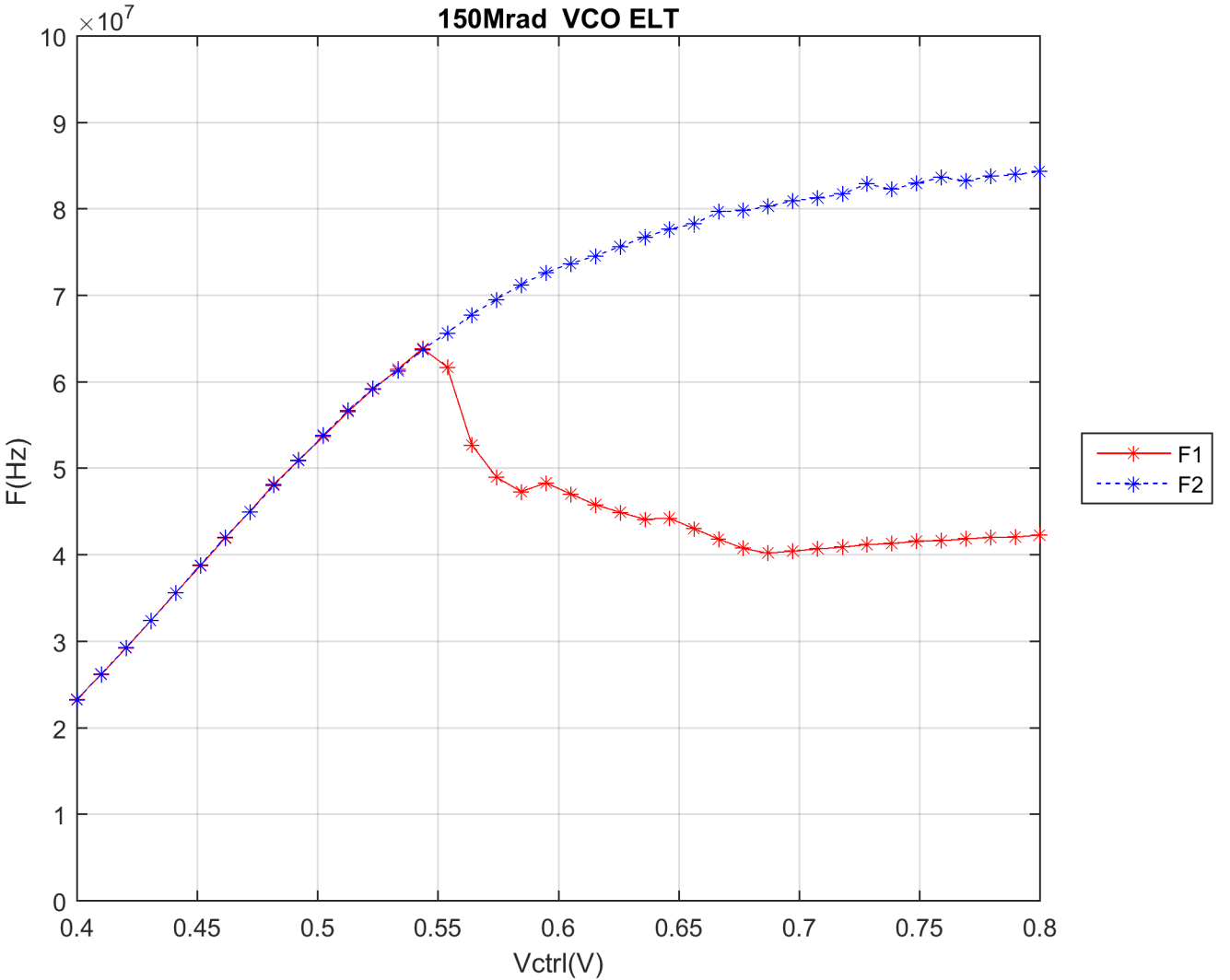
2. Vctrl sweep for ELT transistors VCO (measuring the frequency vs Vctrl).

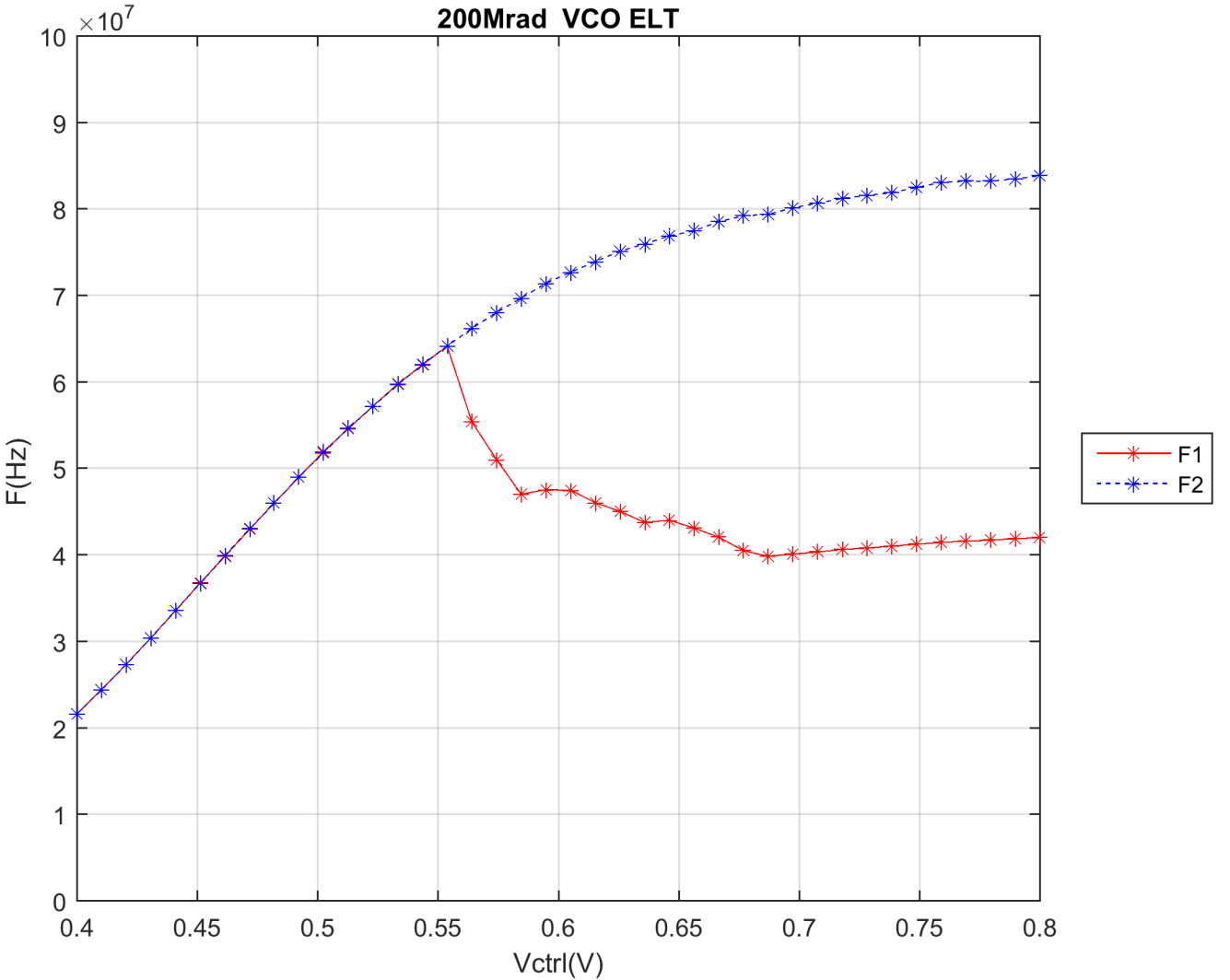

Pre-rad room T VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

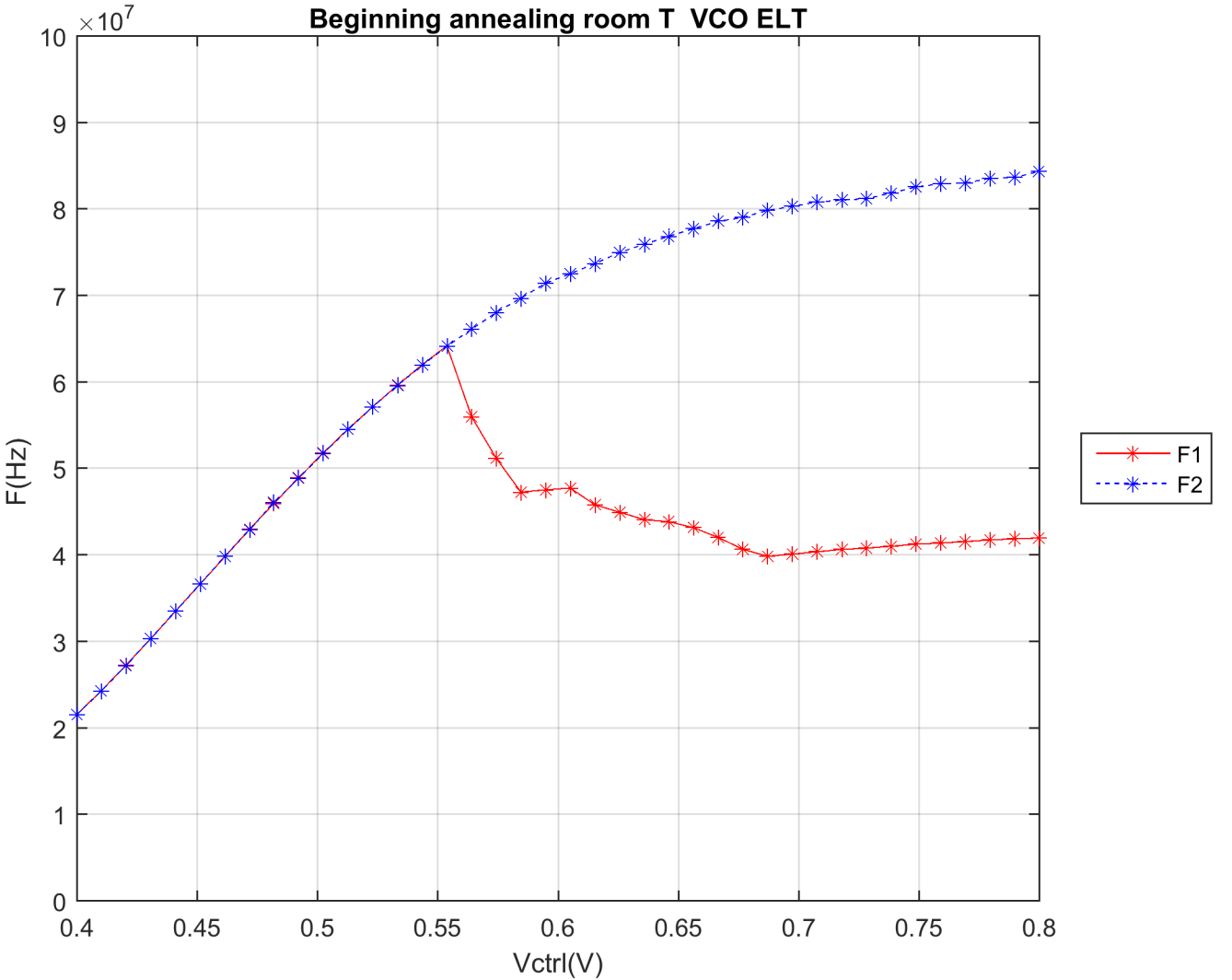

10Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

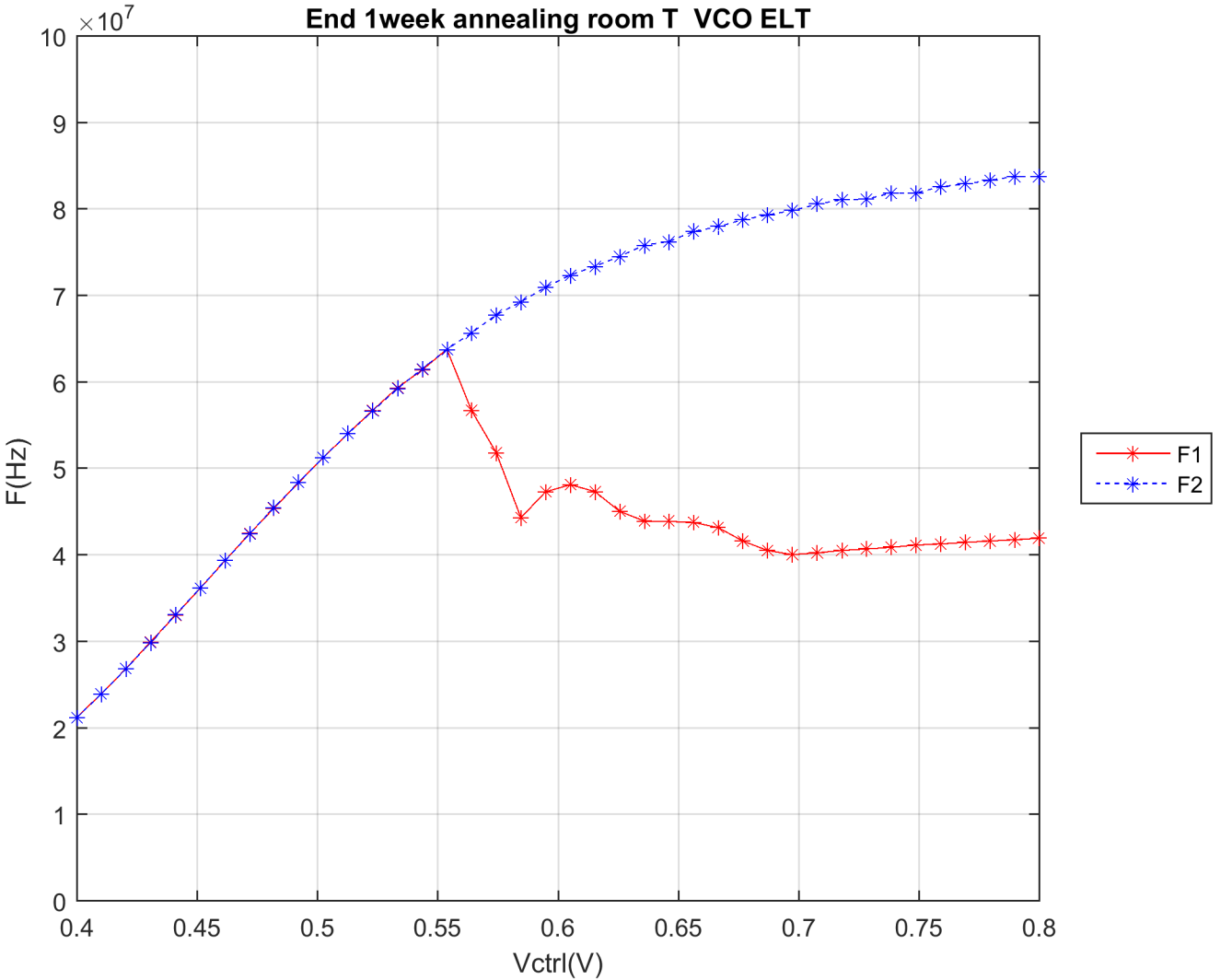

40Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

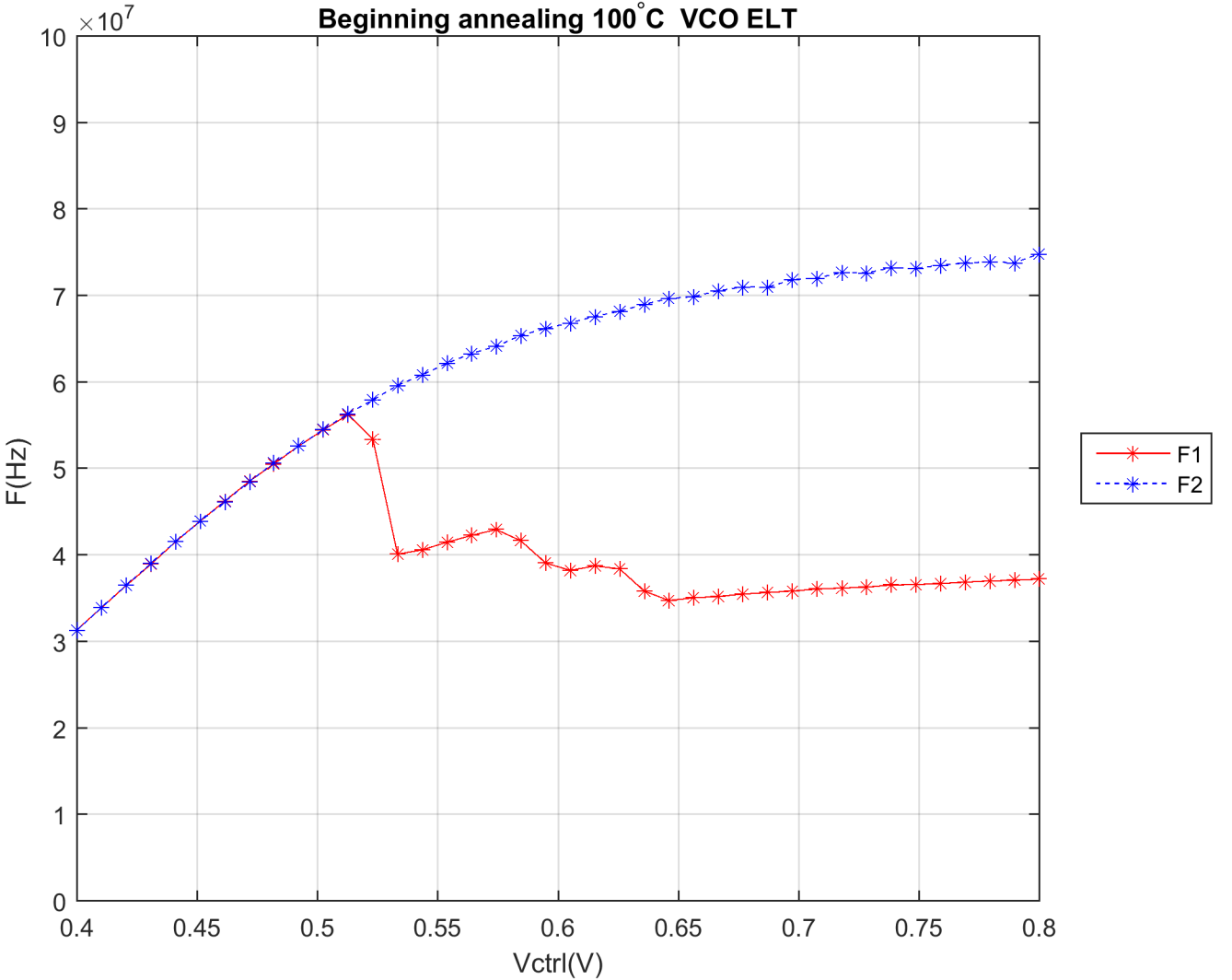

100Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

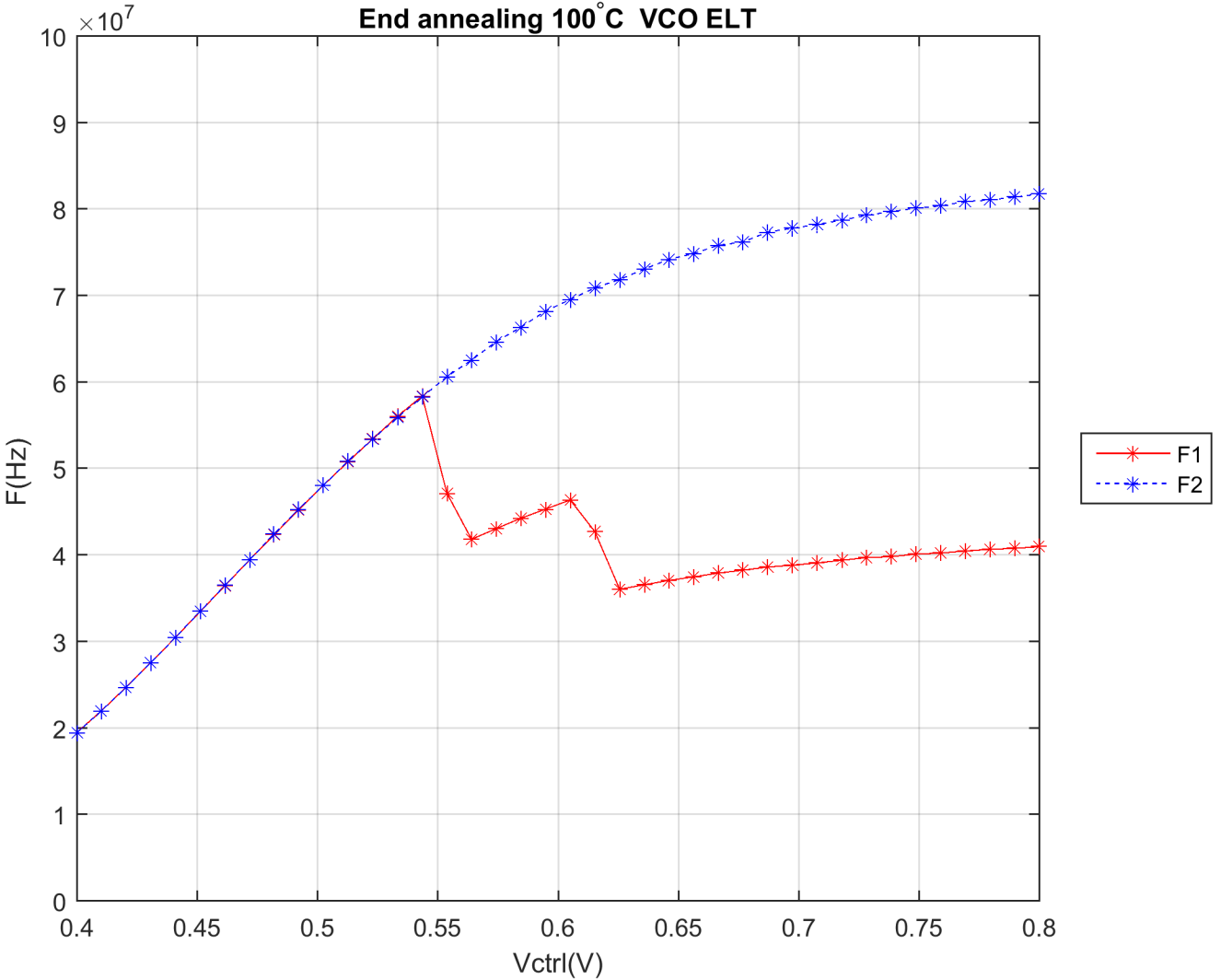

150Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2


200Mrad VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

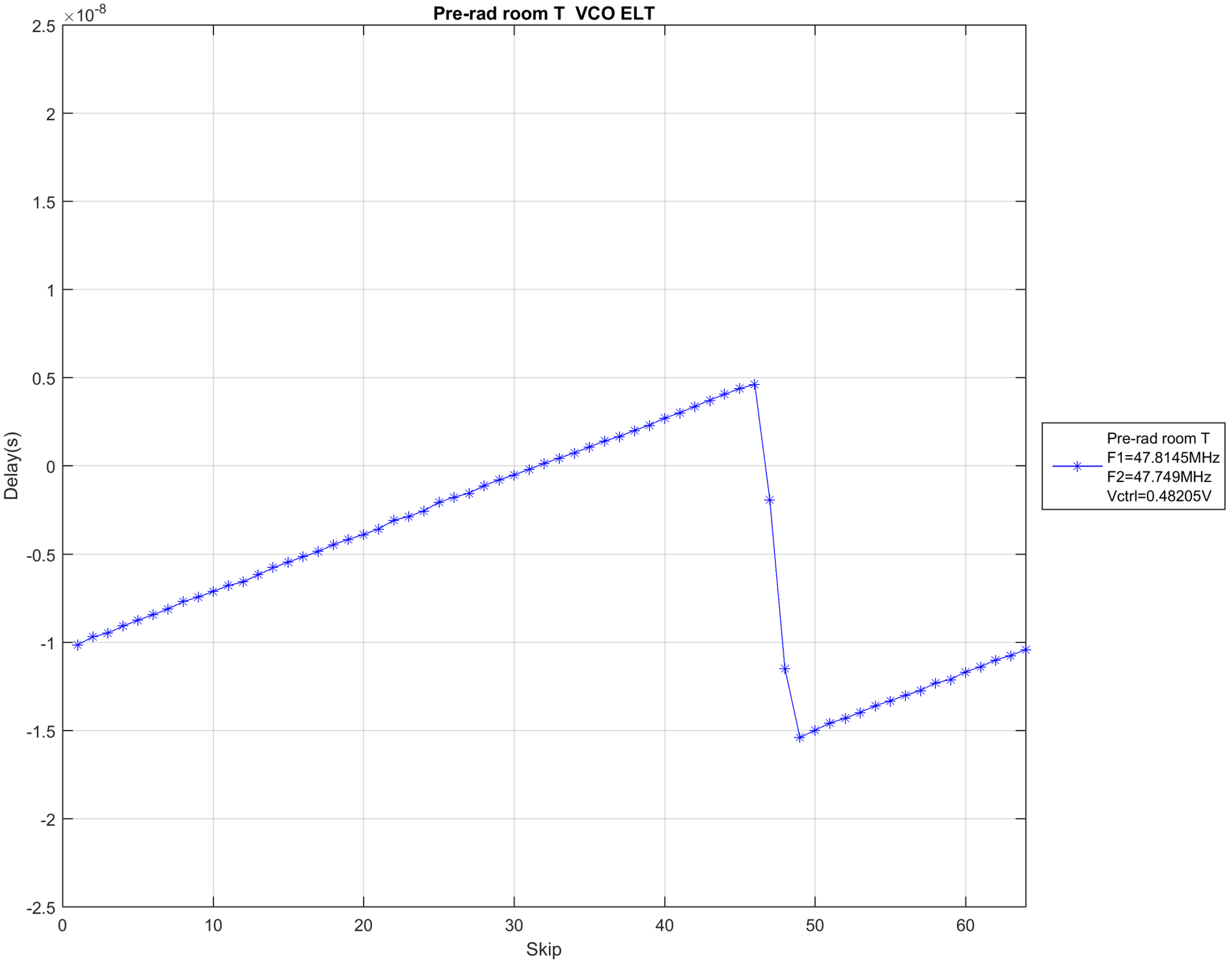

Beginning annealing room T VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

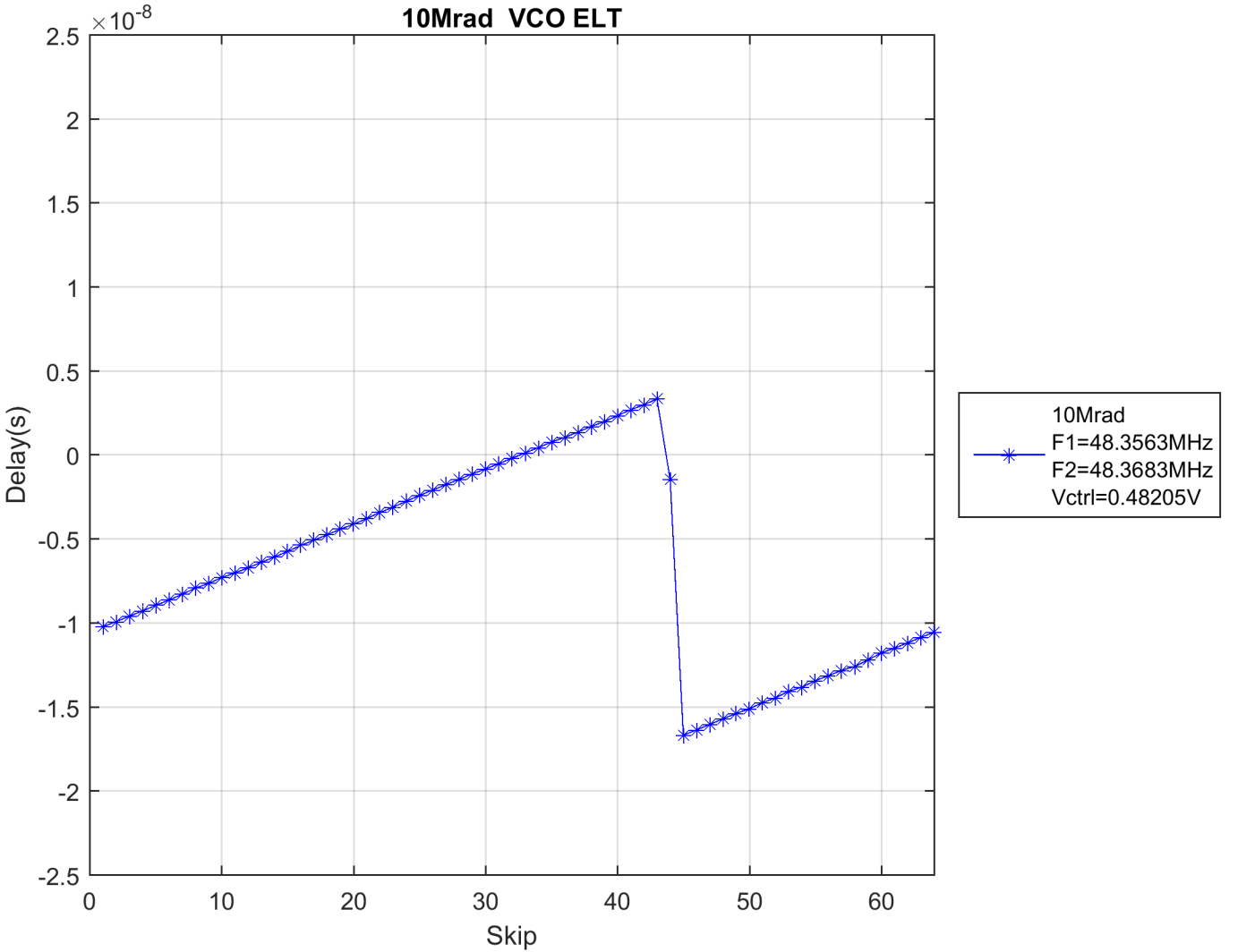

End 1week annealing room T VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

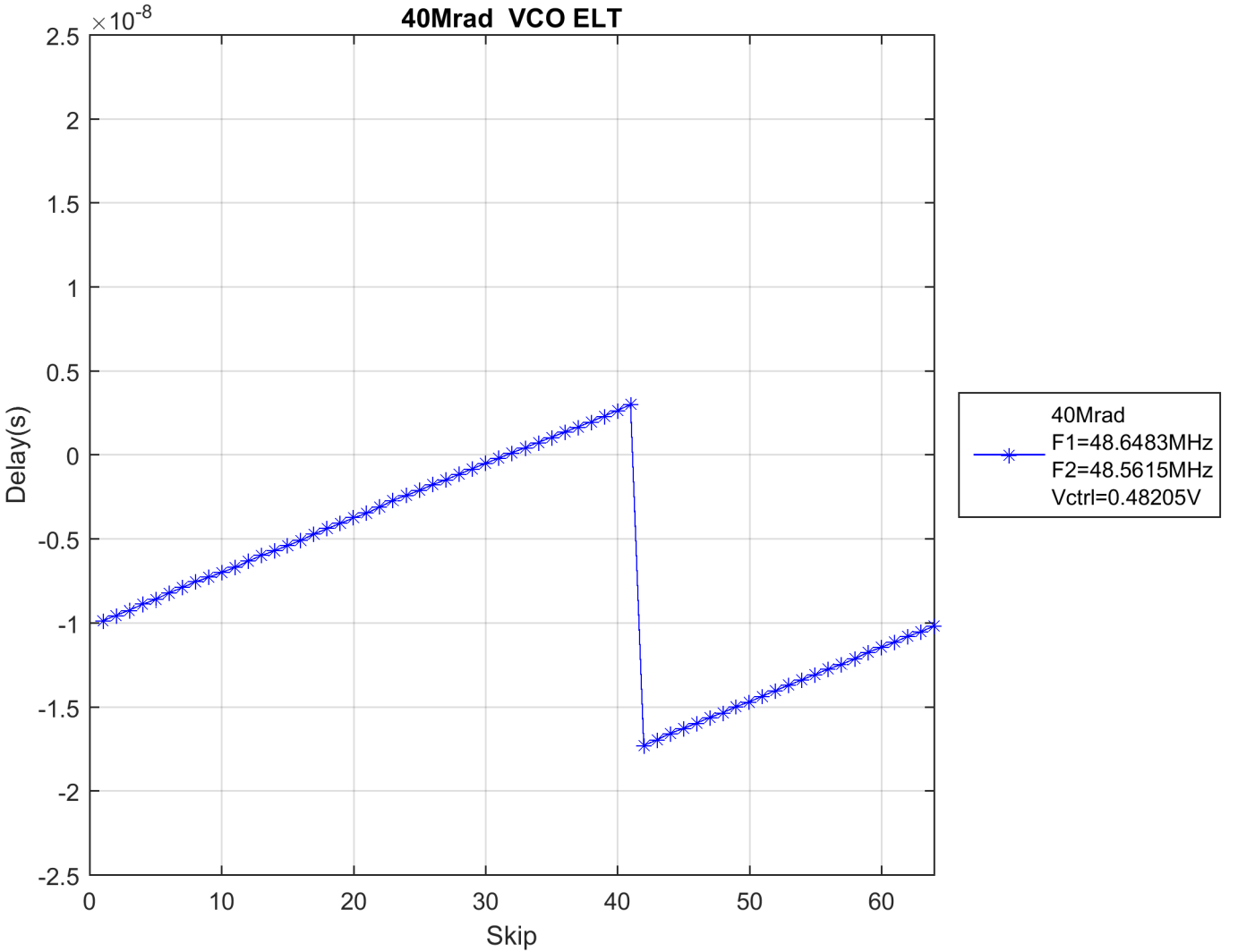

Beginning annealing 100°C VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

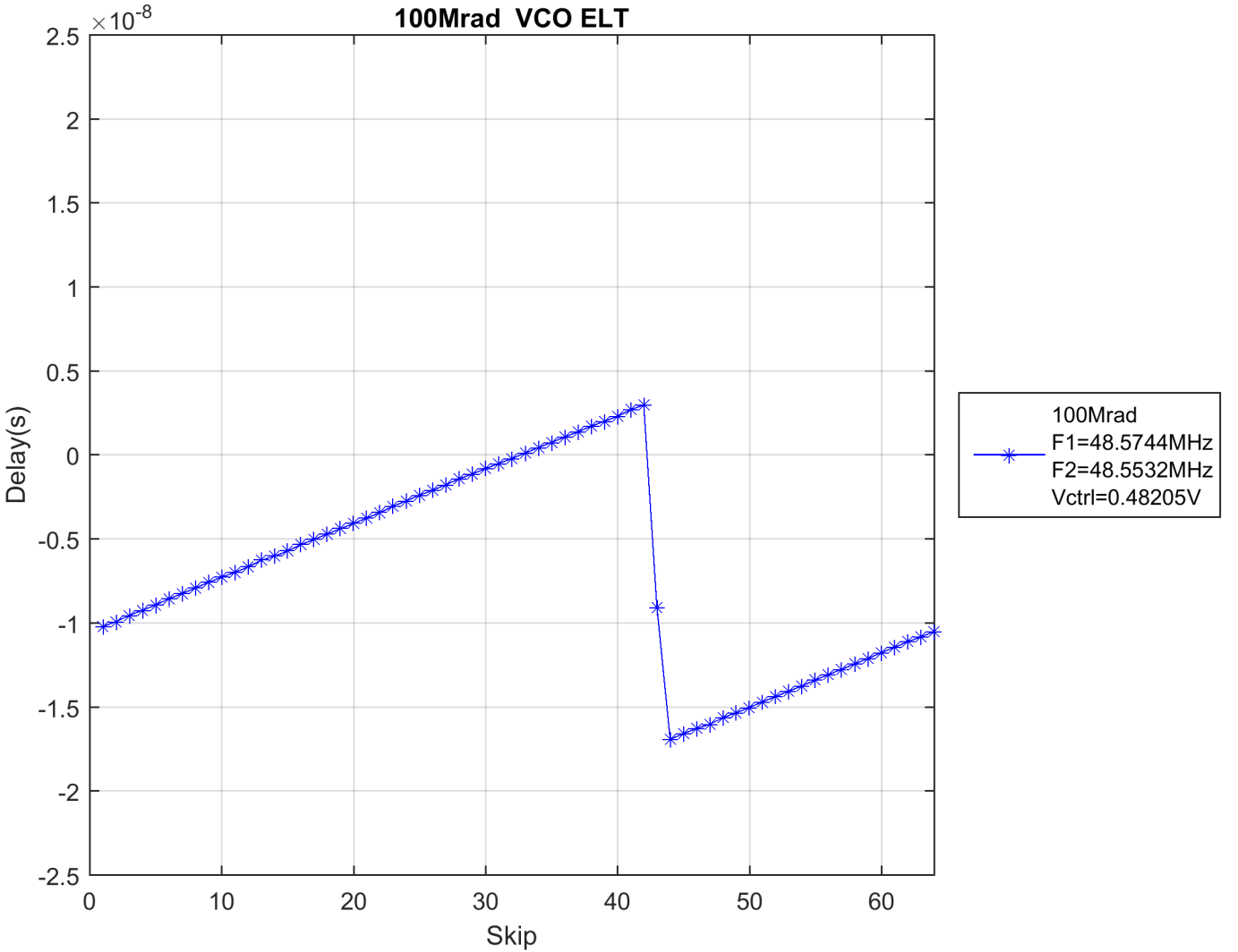

End annealing 100°C VCO ELT
×10^7
10
9
8
7
6
5
4
3
2
1
0
F(Hz)
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
Vctrl(V)
F1
F2

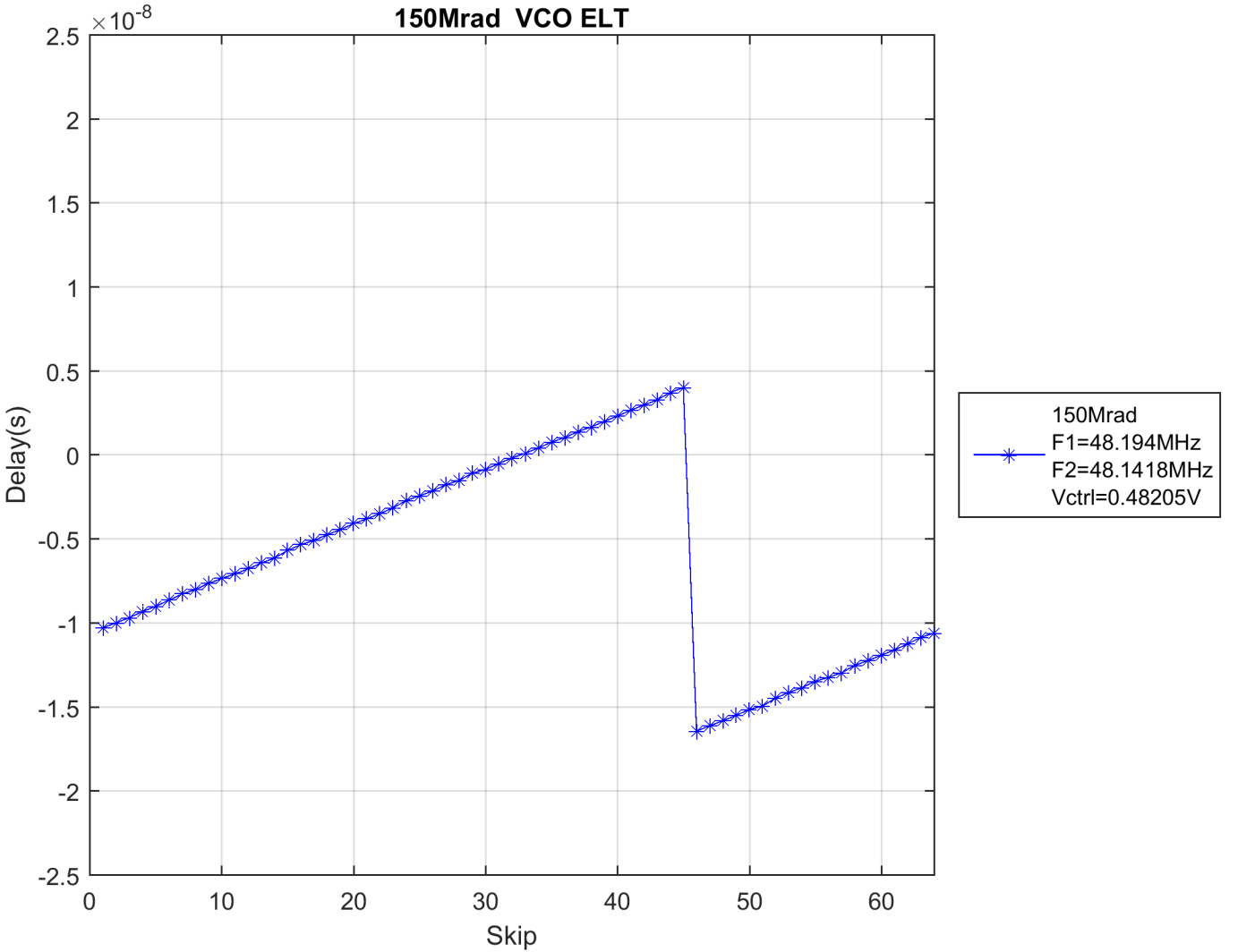
3. Skip test for ELT transistor VCO.

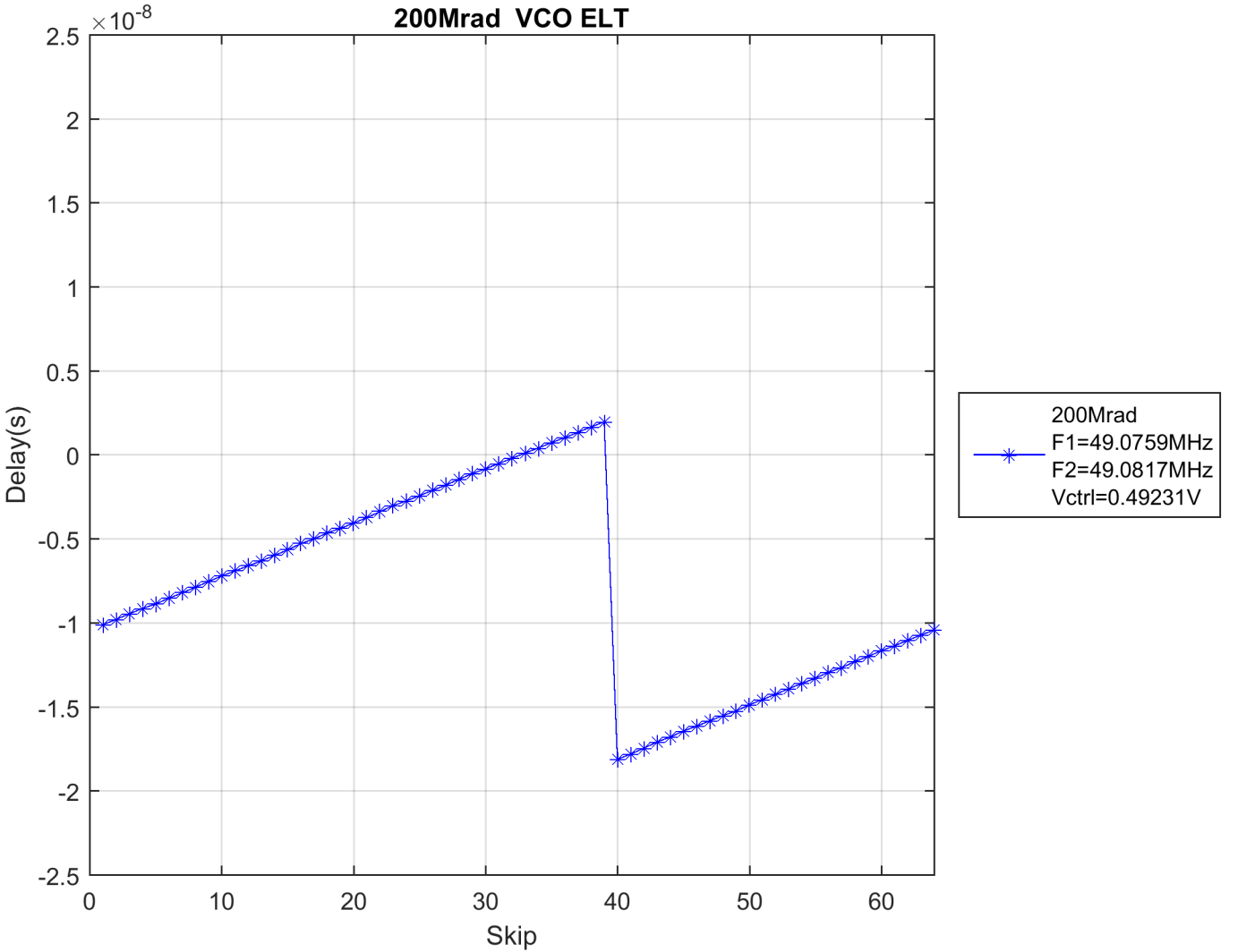

Pre-rad room T VCO ELT
×10^-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
Pre-rad room T
F1=47.8145MHz
F2=47.749MHz
Vctrl=0.48205V

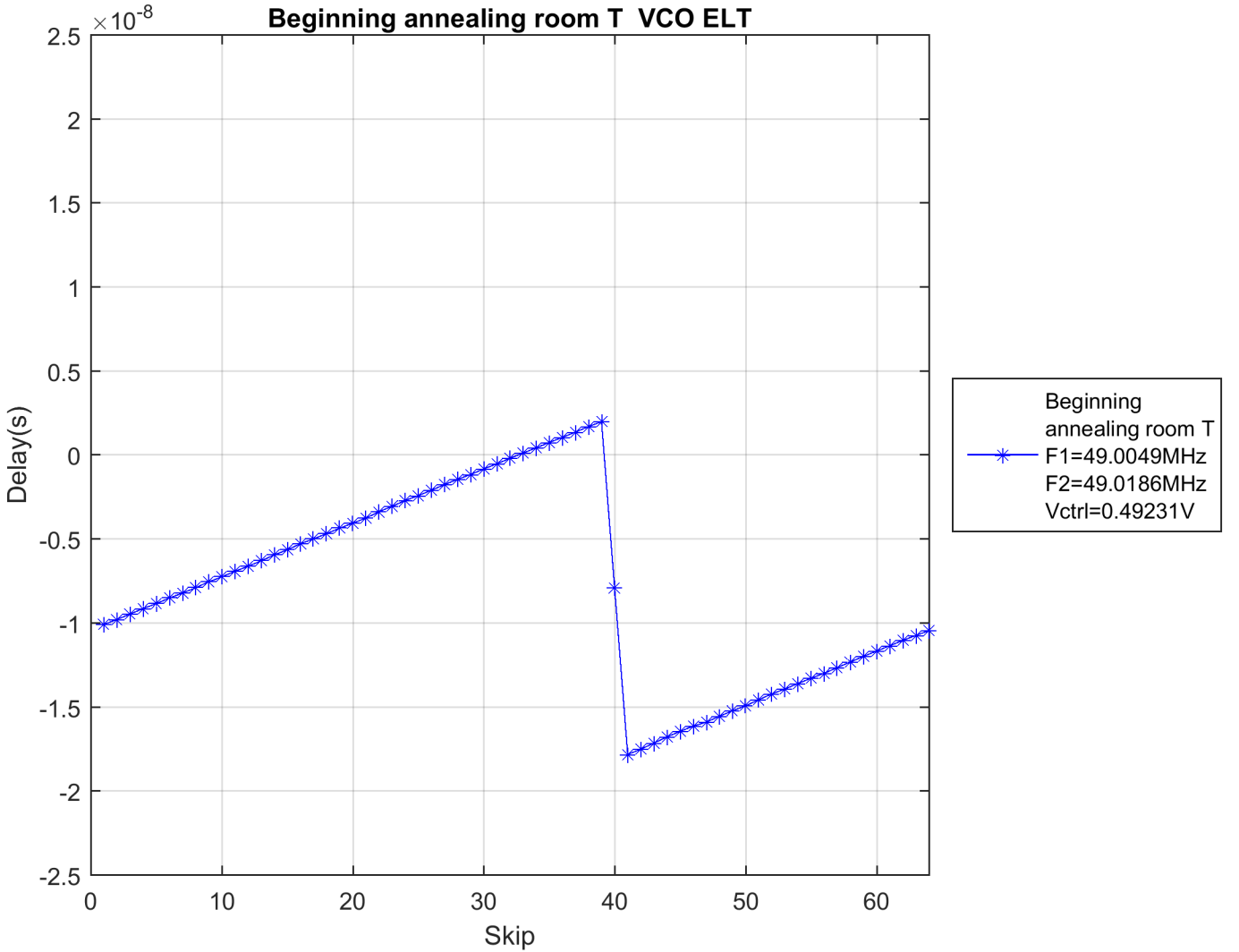

10Mrad VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
10Mrad
F1=48.3563MHz
F2=48.3683MHz
Vctrl=0.48205V

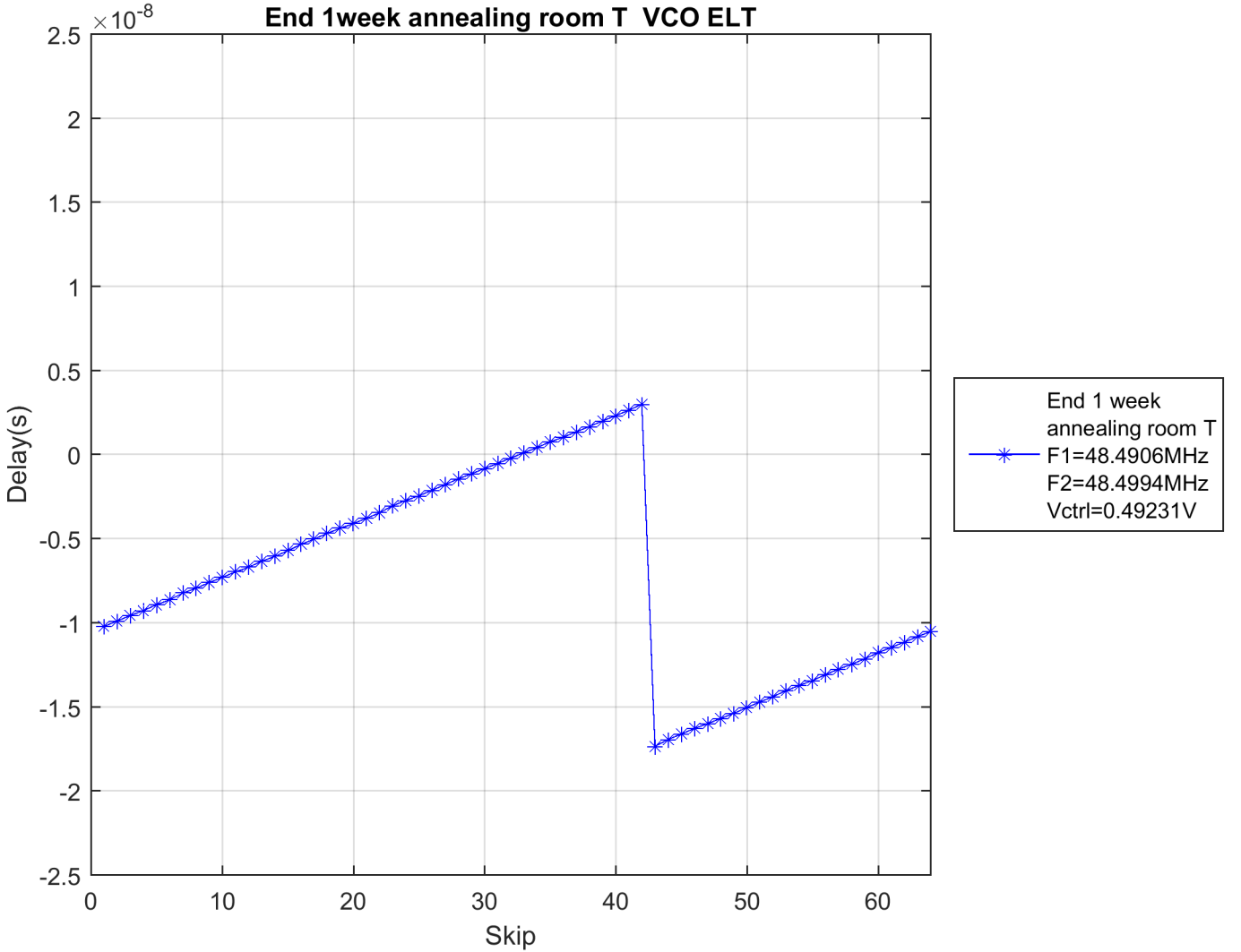

40Mrad VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
40Mrad
F1=48.6483MHz
F2=48.5615MHz
Vctrl=0.48205V

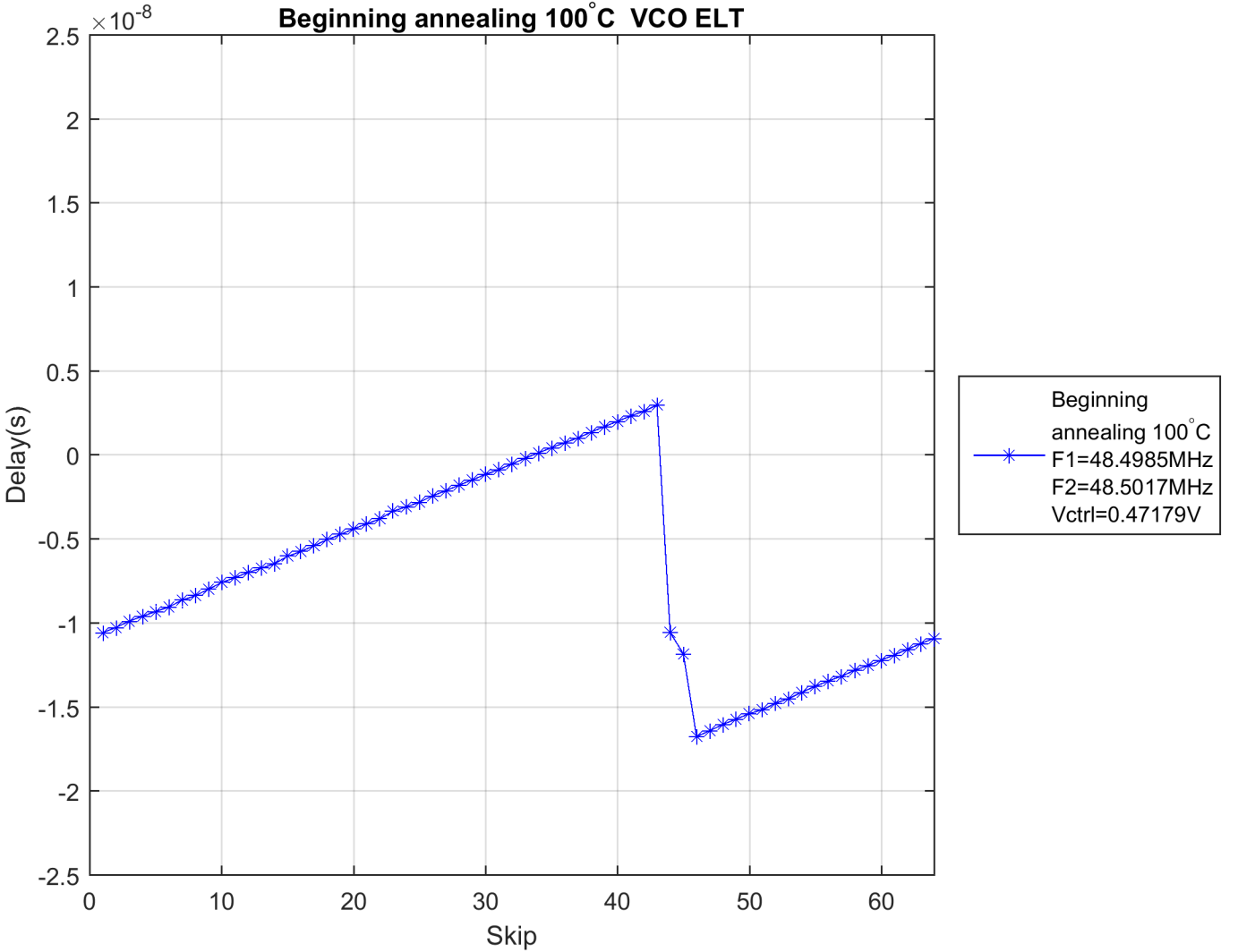

100Mrad VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
100Mrad
F1=48.5744MHz
F2=48.5532MHz
Vctrl=0.48205V

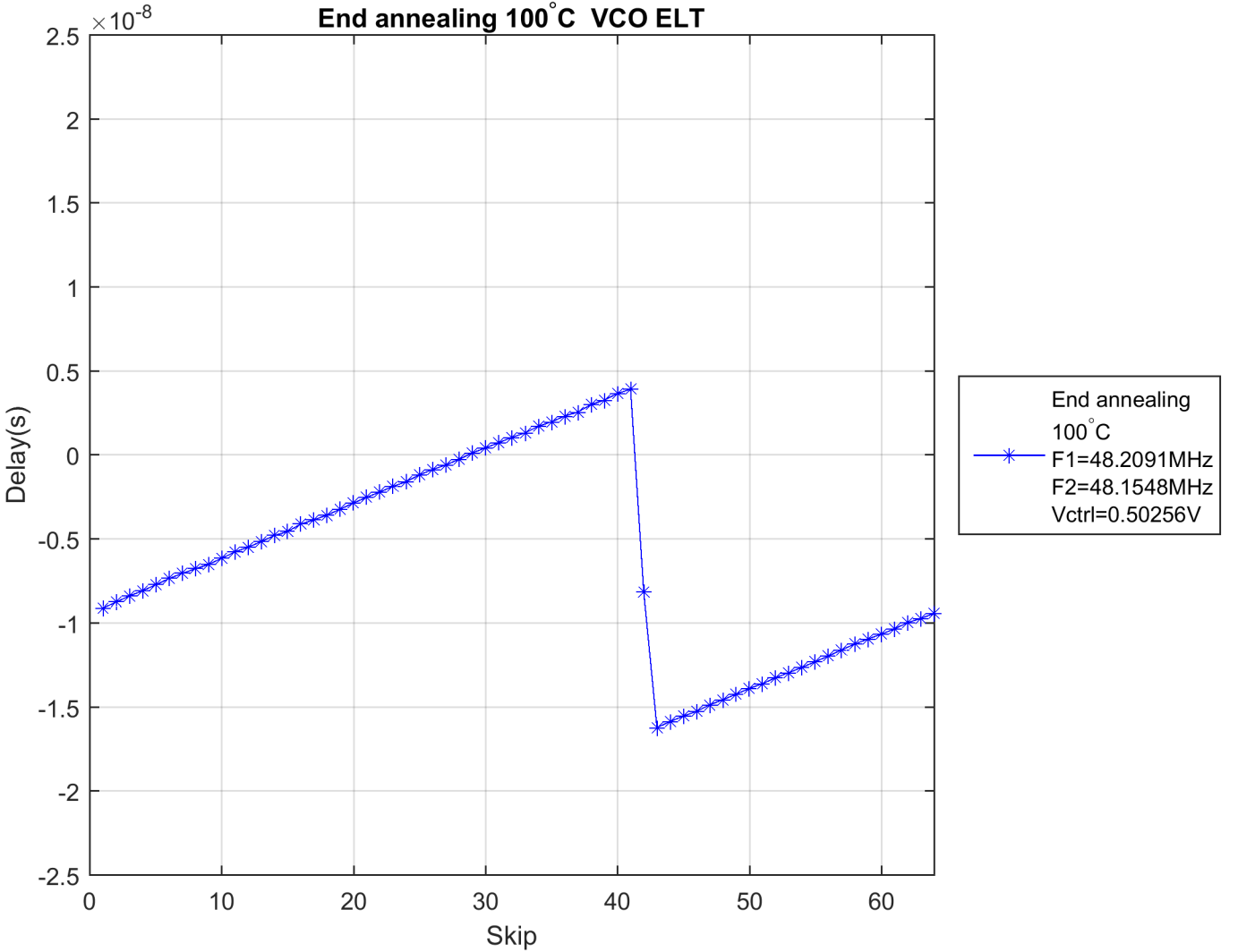

150Mrad VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
150Mrad
F1=48.194MHz
F2=48.1418MHz
Vctrl=0.48205V


200Mrad VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
200Mrad
F1=49.0759MHz
F2=49.0817MHz
Vctrl=0.49231V


Beginning annealing room T VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
Beginning annealing room T
F1=49.0049MHz
F2=49.0186MHz
Vctrl=0.49231V


End 1week annealing room T VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
End 1 week
annealing room T
F1=48.4906MHz
F2=48.4994MHz
Vctrl=0.49231V


Beginning annealing 100°C VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
Beginning annealing 100°C
F1=48.4985MHz
F2=48.5017MHz
Vctrl=0.47179V


End annealing 100°C VCO ELT
×10-8
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
Delay(s)
0
10
20
30
40
50
60
Skip
End annealing
100°C
F1=48.2091MHz
F2=48.1548MHz
Vctrl=0.50256V